Development of an Evaluation Reader for 13.56 MHz RFID systems providing Very High Data Rates up to 6.78 Mbit/s

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***Abstract*— The paper deals with the development of an evaluation reader, based on a field programmable gate array. Due to standardization discussion to enhance the date rate of the actual ISO/IEC 14443 from 848 kbit/s up to 6.78 Mbit/s an evaluation reader is needed, which provides the required signals, as well as field strength. This reader is designed to generate different data rates and modulation schemes, as well as to cover different standards at 13.56 MHz. It is able to test different settings and provides results to optimize those very high data rates.**

I. Introduction

Radio Frequency Identification (RFID) systems have a long history and are part of our everyday's life. Nowadays we get in contact with RFID solutions, even if we don't expect it. In most shops so called Electronic Article Surveillance (EAS) Systems [1] are installed, which protect the products from unauthorized removal from the shop. In some major cities, such as Dhaka [2], London or Moskow, the public transport uses RFID technology for ticketing, as well as to locate busses. Patients in hospitals are marked with a wristband, which is sometimes equipped with an RFID transponder, to be able to store personal data and reduce the risk of malpractice [3].

Those are only a few examples for RFID based applications, which are increasing every day in all areas of life. Beside high frequency (HF) RFID applications, further applications such as proximity coupling devices like the electronic Passport (ePassport) are part of our life. The first generation of the ePassport was introduced in Austria in 2006 and has stored personal data and a picture. In the second generation, which is on the market at the moment, two additional fingerprints are stored on the passport, to be able to compare the passport with the person without doubt. An increase of stored application data volume should come along with even a decrease in the transaction time, to be able to gain the advantage of contactless technology, which is a reduced handling time [4].

Depending on the application, different contactless and RFID systems are available, which work in parallel at different carrier frequencies and operation ranges. This paper focuses on 13.56 MHz RFID systems, which are defined in ISO/IEC 18000-3 [5] or ISO/IEC15693 [6], and proximity coupling devices such as ISO/IEC 14443 [7]. The last one is also included in the International Civil Aviation Organization (ICAO) Document 9303 Part 1 [8], which defines the standards for ePassports. Due to the fact that all new passports are equipped with contactless secure transponders, and the amount of data stored on the chip is increasing, the need for higher data rates is obvious.

In [7] and [9], data rates from 106 kbit/s up to 848 kbit/s are defined. Actually standardization discussions are ongoing to enhance the standard by very high data (VHD) rates up to 6.78 Mbit/s.

This paper deals with an evaluation reader, which allows evaluating different modulation schemes as well as data rates. In the paper a general introduction of RFID systems will be given. The next chapter should give an idea of the motivation, why an evaluation reader is needed and define the requirements. After a detailed description of the hardware, the performance is evaluated and analyzed.

II. Basic Functionality of 13.56 MHz RFID Systems

RFID and secure contactless systems at 13.56 MHz have a wide application field. Even if the applications differ, the basic principle is the same in all HF RFID systems. The principle can be seen in Fig. 1. A reader is the physical interface for a data based operation, e. g. door opener. The reader provides an H-field at the carrier frequency of f_c = 13.56 MHz, which is used to power the transponder, and transmit data, via an air interface.

For the data transmission from the reader to a proximity transponder two different coding schemes are

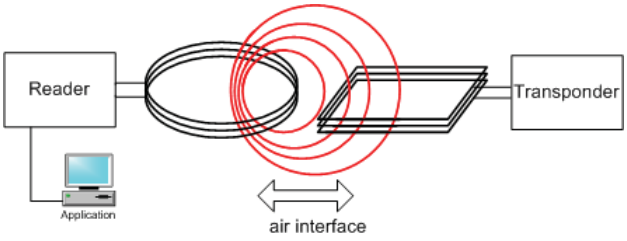

Figure 1. Principle of RFID systems

possible according to [9]. Either the reader is using an 100 % amplitude shift keying (ASK) which is coded with a modified miller code, named Type A. Or transmits its data with a 10 % ASK using an non return to zero code, representing Type B.

Independent of the used modulation scheme, the reader has to provide sufficient energy to power the transponder, since all contactless transponders in proximity coupling devices are passive transponders. This means that they do not have an own power supply, such as a battery. The advantage of this design is that the transponder does not have any parts, which must be replaced regularly. This allows a placement of the transponder in the inner layer of the passport, or in any other closed housing. The transponder takes its energy from the field to power the integrated circuit and performs signal processing. Furthermore the transponder uses the H-field of the reader to transmit the information back to the reader. This is done by load modulation. Since the transponder is powered by the H-field of the reader, it does not have the possibility to transmit data in an active way. By switching a load modulator, which can be a transistor or a switch and a resistor, according to the data which should be transmitted, the transponder changes its impedance. The impedance change causes a change of the quality factor of the transponder, which influences the H-field of the reader. Due to these changes of the field, the reader is able to extract the data from the transponder.

III. Motivation

In [7] and [9] data rates up to 848 kbit/s are defined and currently standardization discussions are ongoing to increase the data rate up to 6.78 Mbit/s. The problem is that there are several possible ways to increase the data rate to the desired speed. One option would be to extrapolate the existing specification for higher data rates. The data rate is increased from 106 kbit/s to 848 kbit/s by reducing the symbol time. Extending the data rate according to this method, the required bandwidth is increased continuously as described in [10].

Considering frequency regulation [11], this way of increasing the data rate will violate the spectral mask for emissions. Furthermore due to the system and to be more energy efficient, the reader antenna circuit as well as the transponder antenna circuit has a certain quality factor (Q). The reader antenna resonance circuit is tuned to the carrier frequency (f_c) of 13.56 MHz, to be able to emit a maximum H-field strength from limited amplifier output and supply power. Increasing the power efficiency means increasing the quality factor. The transponder is tuned to a resonance frequency between 14-18 MHz, not to influence the reader too much [12]. A boost in H-field strength means a limiation in bandwidth (BW) according to Eqn. 1.

$$BW_{3dB} = \frac{f_c}{Q}. \tag{1}$$

This means that an increase of the quality factor, which is increasing the energy efficiency, results in a reduction of the provided modulation bandwidth and in an increase of the time constant, which causes inter symbol interference.

Furthermore the coupling factor, which describes the relation between two coils, changes with the geometry of the coils, the distance and the orientation. This also results in detuning effects, which shift the resonance frequency and have impact on the quality factor.

To be able to get accurate results with all different settings, an evaluation reader was developed.

A. Requirements

The development of the evaluation reader has a very extensive list of requirements. The reader should have the highest degree of freedom. That means that it has to allow to attach different antennas to the amplifier of the reader, to show the influences of different antenna properties on the system.

It has to be possible to generate commands at the base data rate of 106 kbit/s according to [7], which is needed for the initialization of higher data rates up to 848 kbit/s, as well as in Type A as Type B. Furthermore different VHD options have be manageable, such as the phase shift keying (PSK) interface as well as the ASK interface option for reader to card communication, according to the current draft standard specification. Table I gives an overview of the data rates and modulation schemes, which have to be generated with the evaluation reader. To be able to generate all those signals and to amplify them, the whole structure has to have a certain bandwidth, which has to be considered in the development. For the PSK modulation an additional option has to be implemented to be able to reduce the angle, between the symbols in the constellation plot. In classical PSK modulation, the constellation points are located around the whole circle. For example the 8 PSK has a constellation point at 0, $\pi/4$, $\pi/2$,... which fills the whole circle. The problem in this case is according to [10], that the emmitted spectral bandwidth changes, and not enough energy is transmitted at the carrier. To avoid this problem and to transmit more energy at the carrier frequency, the used angle can be reduced. Instead of using the complete circle, the constellation points are located for example in a segment between 0 and $\pi/3$. To be able to find the best angle, as well as to prove different considerations, it must be possible to change the modulation angle.

The evaluation reader must have the ability to provide enough power to allow data transmission with different

TABLE I
Achievable data rates [kbit/s]

symbol time	ASK Type A/B	2PSK	4PSK	8PSK	16PSK
128/fc	106	-	-	-	-
64/fc	212	-	-	-	-
32/fc	424	-	-	-	-
16/fc	848	-	1695	2542	3390
8/fc	1695	1695	3390	5090	6780
4/fc	3390	3390	6780	10170	-
2/fc	6780	6780	13560	-	-

antennas and quality factors. As defined in [7], a field strength between 1.5 and 7.5 A/m has to be achieved.

Furthermore the platform has to have a receive path, to receive the answer from the transponder to have full reader functionality for demonstration.

Our reader also offers an output, to control the load modulator (LM) at the transponder, to allow to perform stand alone bit error rate (BER) measurements with the reference proximity integrated circuit card (PICC) defined in [13].

IV. Evaluation Platform

The VHD evaluation reader consists of 4 main parts, which are depicted in Fig. 2. The basic of this evaluation reader can be found in [14]. To have the highest degree of freedom, the evaluation reader is based on a field programmable gate array (FPGA) board to generate and evaluate the digital part of the evaluation reader. The Virtex 5 Xilinx commercial evaluation board, is marked in the Figure with A. B is the adapter board to connect the FPGA to the converter C, which contains the analog to digital converter (ADC) as well as digital to analog converter (DAC). On D, the evaluation board, the analog components of the evaluation reader are located.

The Virtex 5 evaluation board ML507 is separated in 4 functional blocks, as depicted in Fig. 3. A receiver is located on the evaluation board, which receives the input of an ADC. The signal processing can be done either on the evaluation board itself, or the data can be raw sent over an Ethernet connection to a computer for signal processing. The communication to the PC is needed to control the evaluation board, send data to the transmitter as well as to receive the data from the receiver. The transmitter of the reader is generating the required signals, such as carrier or modulated signal, either using ASK or PSK. This signal is transformed to the analog domain by a DAC.

Additionally a transmitter for the transponder is located on the evaluation board, to allow stand alone BER measurements for the communication of the transponder to the reader. Therefore the LM of the transponder can be controlled by the evaluation board, and allows different

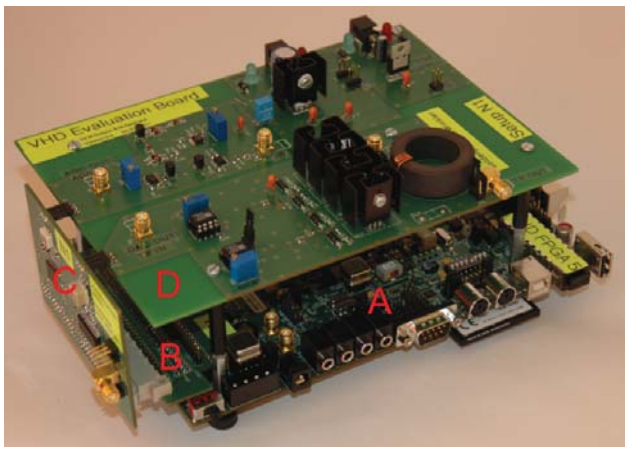

Figure 2. VHD evaluation reader

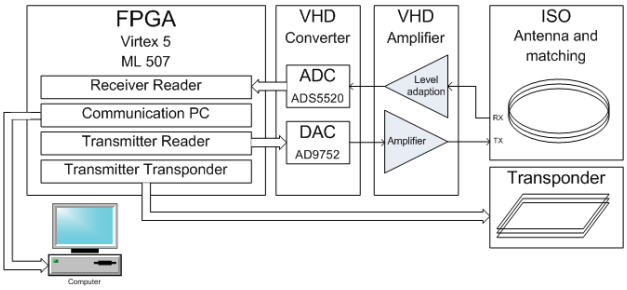

Figure 3. Block diagram of the evaluation reader

data rates, as well as modulation schemes.

The output of the DAC is amplified by an amplifier in several steps, to achieve the required H-field strength. Furthermore the input of the ADC is controlled by an automatic gain control (AGC) circuit, to efficiently use the dynamic range of the ADC and protect it from overload.

A. Digital Unit - FPGA

The VHD evaluation reader is based on the commercially available Virtex 5 FPGA, which is embedded in the ML507 evaluation platform of Xilinx. This board was chosen because of its availability and flexibility of options it offers. It is possible to generate all kinds of signals, and with the embedded power PC it offers a wide range of applications. With the developed converter board and the according amplifier it is possible to generate different protocols and signals shapes, such as for [5], [6] or [7]. According to this flexibility of the ML507 board it is a useful tool for digital designers and software engineers, who deal with contactless technologies.

Beside the FPGA, the platform provides several digital interfaces such as USB, Ethernet, RS232 or DVI. Furthermore there are several clock domains, to allow the user to generate a clock at any frequency up to 550 MHz.

In Fig. 4 the ML507 is shown, and the relevant parts are marked in the picture. The RJ45 Ethernet connector (A1) is used for the communication between the reader and the PC, to control the evaluation reader and transmit test data. On the one hand configuration settings for the contactless communication interface are transmitted to the FPGA, for example to change the data rate or modulation scheme. On the other hand, received data, which are sampled with the ADC, are transmitted to the PC to allow post processing in Matlab or any other program.

A2 is the JTAG interface, which is used to program the FPGA. There is the opportunity to program the FPGA, via the JTAG interface. Another option is to load the program on the flash card, as a card slot is available at the bottom of the ML507 board. One of these options can be selected by DIP switches on the board itself.

Due to the fact that the FPGA chip itself heats up during measurement and to prolong its lifetime, it is hidden behind a fan (A3), which is mounted directly on the IC.

To generate the carrier field, the 100 MHz PLL on board, which is plugged at A4 is replaced by an harmonic

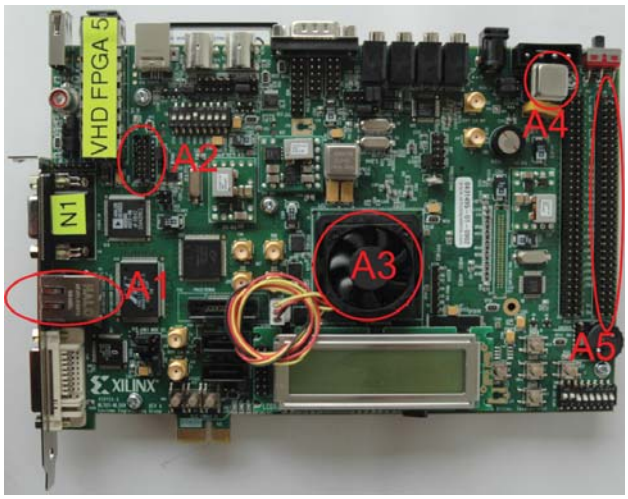

Figure 4. FPGA board ML507

crystal oscillator providing 108.48 MHz. Dividing the clock by the factor of 8 results in a carrier frequency of 13.56 MHz. That means each carrier period can be defined by 8 points. If only a carrier field is generated, a counter addresses a look up table (LUT), which contains the amplitude information of a single carrier period.

The realization of the ASK modulation can be done by a multiplier after the LUT, to change the amplitude level, or by an additional LUT with different amplitude levels. For the generation of the PSK, the LUT could be enhanced, to allow the amplitude to start at any level. Furthermore a LUT with the I and Q value of the symbols can be implemented, and the output is generated by an IQ modulator. Independent of the generation of the signal, it has to have 12 bits resolution, to be transformed into the analog domain.

With this high degree of freedom, all different signals, coding schemes and data rates can be generated.

As interface to the analog environment the IO connector at A5 is used. There are 32 IO pins, which can be defined by the user and additionally there are some supply pins, which provide 5 V and 3.3 V, which are used to supply the converters.

B. Adapter

The adapter connects the ML507 board to the converter. To use the VHD evaluation reader as demonstrator for VHD rates, the setup should be compact. An adapter was developed to connect the IO pins of the ML507 board to the converter board, which is mounted vertically and connects the ML507 board to the analog amplifiers. By placing the converters in the vertical plane, the digital wires can be kept as short as possible. This reduces distortion on the digital signals, as well as in the analog domain. The digital signals operate at 108.48 MHz, so longer wires would form antennas and distort the good analog performance.

Furthermore the adapter combines the IO pins from the ML507 board, the ground (GND) and supply voltage to a connector, which can be easily connected to the converter. Finally the differential pins from the ML507 board are connected to a pin connector on the top of the adapter. These pins are used as debug pins for ML507 board programming and can also be used to provide additional signals for measurements.

C. Converter

The converter is located in the vertical part of the platform and is used to convert signals of the analog domain into the digital domain and vice versa.

On the left side of Fig. 5, the ADC can be seen. The ADC chip is an ADS5520 produced by Texas Instruments. With its 12 bit resolution it fits perfectly in the concept of the reader, and has a voltage resolution below 0.6 mV. Another benefit of this converter is the single supply voltage of 5 V. That way the ADC can be supplied by the ML507 board and no further power supply is required. The ADC has a maximum sampling rate of 125 MS/s, but is clocked in this application with the system clock of 108.48 MHz. Since the ADC has a differential input, but the AGC is only working with a single ended signal, a transformer is used to transform the single ended input to a differential one. Furthermore the transformer separates the ground from the ML507 board and the evaluation board.

The middle part of the converter hosts the DAC. It is an AD9752 produced by Analog Devices. It is possible to generate all kinds of signals in the digital domain on the ML507 board and transform it to the analog domain with the help of this converter. With the maximum sampling frequency of 125 MS/s, and 12 bit resolution, the converter is ideal to generate the carrier, as well as different ASK and PSK modulated signals with high accuracy. The clock is the system clock of the ML507 board. The DAC requires a power supply of 3.3 V and 5 V, which are both provided by the ML507 board. Since a differential output is provided, a transformer is used to combine the differential output to a single ended output, and decouples the ground from the ML507 board and the evaluation board.

This contactless reader evaluation board also includes an option to generate the transponder load modulation signal. For this purpose on the right side of the board

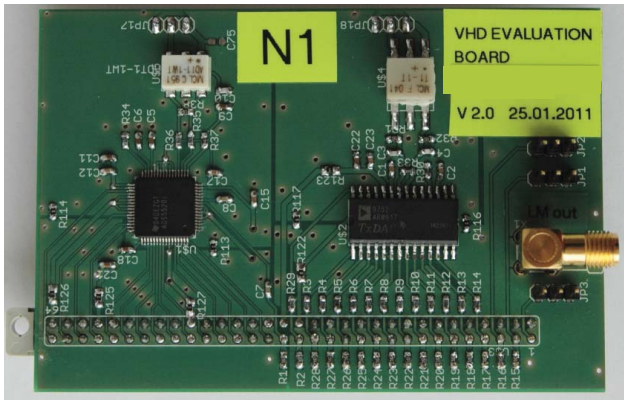

Figure 5. VHD converter board

different connectors can be found. JP3 and the SMA connector are the LM output. This signal is used to control the LM on the card side, if the evaluation reader is used to test the communication of card to reader. For this scenario, the ML507 board generates a carrier field, and provides an LM control signal. The received data are sampled at the ADC and a BER calculation can be done.

The outputs of JP1 and JP2 can be used as toggle signals to indicate a new period, signal, trigger or anything else needed for measurements.

While designing the converter board a main focus was put on the ground plane of the converter. Due to the high frequency of the digital signals and the sharp edges, they induce distortion in the ground plane. Especially at the analog part of the ADC, it is important to guarantee a stable ground plane, since the signal, which should be detected, has a very small voltage variation. Each additional distortion can lead to wrong decisions at the receiver. To keep the ground as stable as possible, 4 separated ground domains were implemented. The digital part of the ADC, as well as the DAC have a seperate ground plane, which are connected at the connector to the ML507 board. The digital signals for the LM and the toggle signals are connected to the ground plane of the DAC.

The analog ground plane of the ADC and the DAC are separated and connected to the related converter. The ground planes are connected at two points, and stabilized by capacitors to the supply voltage. Due to this separation of the ground planes, the influence of the digital part can be minimized.

Furthermore the transformer at the output of the DAC respectively the input of the ADC decouples the converter board from the evaluation board. That way there is no ground connection between the converter and the ML507 board, and the evaluation board. This means that no ground loop can be built between the power supply of the FPGA and the power supply of the evaluation board, which leads to a more stable behavior.

Finally as few signals as possible were routed on the bottom ground plane of the converter. Due to the few interruptions of the ground plane, it is used as electrical shield to avoid distortion to the amplifier, as well as on the ML507 board.

D. Evaluation Board

The VHD evaluation board has several functional blocks, as depicted in Fig. 6. Connectors to the converter board are placed on the left side. The 4 parts on the board are separated into the transmit amplifier (1), the AGC for the receive path (2), the power supply unit for the printed circuit board (PCB) (3) and an additional supply unit for the ML507 board (4), which is implemented for future use, in case the evaluation reader should be used for demonstrations, and be supplied by a single external supply.

1) Transmit amplifier: To be able to generate the signals, which are required for [7], the amplifier has to generate an H-field of up to 7.5 A/m field strength

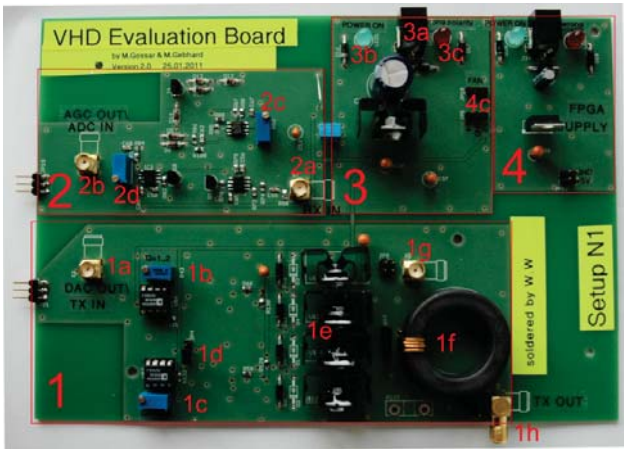

Figure 6. VHD evaluation board

(H), at a distance (x) of 37.5 mm. The used antenna is standardized in [15], with a quality factor (Q) of 35, a radius (r) of 7.5 cm and one turn (N). The antenna has an inductance (L) of 480 nH. According to Biot-Savart (Eqn. 2), the current (I) in the antenna conductor has to be 1.57 A, taking the parameters above.

$$I = \frac{H\sqrt{r^2 + x^2}^3}{N\,r^2} \tag{2}$$

The required output power (P_0) of the amplifier is calculated based on the required current and the antenna parameters with Eqn. 3.

$$P_0 = \frac{2\pi f_c L I^2}{N^2 Q}, \tag{3}$$

The input of the antenna is matched to $R = 50\Omega$, which means that the required voltage (U_{rms}) can be calculated by Eqn. 4.

$$U_{rms} = \sqrt{R\,P_0^2} \tag{4}$$

With impedance matching this means that the amplifier has to have an output voltage of around 67 Vpp in the unloaded case. To be able to achieve this voltage, the amplifier would require an supply voltage of more than $\pm$ 35 V. To reduce the required input voltage of the amplifier, a four quadrant amplifier with a balun is used. Due to the fact that 24 Vpp are more common, a lower output power will be accepted for the first version of the amplifier. Due to the requirements, the transmit amplifier is built in several steps, as will be explained in the following part, and is depicted in Fig. 7.

The analog output signal of the DAC is connected to the amplifier, with the help of the pins which are placed on the left bottom side.

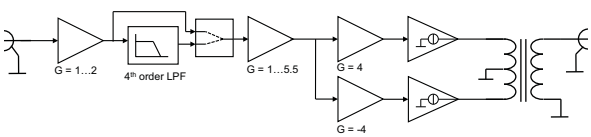

Figure 7. Transmit amplifier block diagram

To be able to use the amplifier without ML507 board, or to be able to observe the output of the DAC, it is possible to use the connector (1a). This connection is used to test the amplifier as well as to use the amplifier in combination with other signal sources.

The first amplifier stage guarantees that the output of the DAC is not over loaded. Using the variable resistor (1b) the gain can be adjusted between 1 and 2. This first voltage amplifier, which comprises an integrated broadband amplifier of Analog Devices is followed by a multi feedback 4^{th} order active low pass filter. This filter should reduce the voltage steps which are caused by the DAC and smoothen the signal. The low pass filter has a cut off frequency of about 27 MHz, which allows to generate a carrier field, as well as different modulated signals, such as ASK and PSK, without bandwidth restrictions. After filtering the signal it is amplified again by a factor between 1 and 5.5, which can be adjusted by the variable resistor (1c). For certain evaluation measurements it is a benefit, if the filter can be removed, and therefore a jumper (1d) allows to bypass the filter very easily.

The next part is a high voltage broadband amplifier requiring 24 V supply. It is possible to supply the amplifier with up to 30 V, but as mentioned before, it is more common to use 24 V. To be able to get a higher output voltage, the amplifier is implemented as four quadrant amplifier, with two separate paths, as depicted in Fig. 7. The first one uses a high voltage non-inverting amplifier at a gain factor of 4 as depicted in Fig. 8, and a second path uses an inverting amplifier of the same gain. Due to the high voltage amplification it is very critical to prevent the amplifier from oscillating. Therefore the feedback loop is designed as short as possible, and the power supply of the amplifier is stabilized close to the amplifier. Not to influence the power supply of the second high voltage amplifier and the current amplifier, which are also supplied by the same 24 V power supply, the input is decoupled by a low ohmic resistor (R1), and stabilized by two additional capacitors (C2 and C3) close to the amplifier, as can be seen in Fig. 8. Since the power supply is single ended, an offset has to be added to the signal, not to cut one half wave of the signal. Therefore the offset of 6 V from the first stage, which is operating at 12 V, is removed by an input AC coupling capacitor (C1), and a voltage divider, which adds a 12 V offset. This voltage divider consists of 2 10 kOhm resistors (R3 and R4) and is decoupled from the power supply by a 47 Ohm resistor (R2) and the node between this resistor and the voltage divider again is stabilized by 2 capacitors (C4 and C5). That way any voltage ripple of the supply voltage is decoupled and the input is stabilized. Additionally the feedback loop is decoupled from the ground potential by a capacitor (C6), since the input is not referred to ground (GND).

The high voltage amplifiers allow to drive an output current of 300 mA. Not to overload them, the amplifiers are followed by a current amplifier (1e), to allow a higher output current.

To combine the differential signal to a single ended

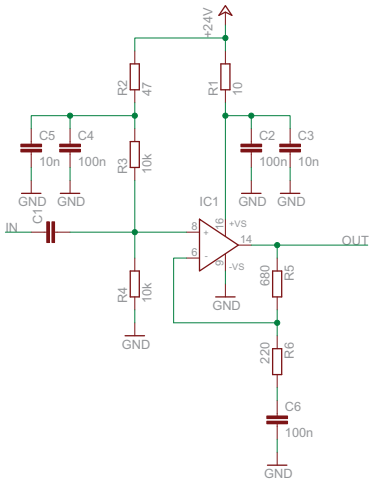

Figure 8. High voltage amplifier circuit

signal a broadband ferrite balun (1f) is used. To have a more flexible structure, the balun can be disconnected, and the separate paths can be connected to the output SMA connectors (1g) and (1h). If the balun is used, the signal is sent to the output (1h), where the antenna is connected.

2) Receive path: The receive path (2) consists of an AGC circuit. It was defined to implement an AGC as input structure, to be able to change the output power of the amplifier, without the need to take care of the input voltage. Furthermore the receive path is connected to the damping factor reducing resistor at the antenna. Depending on the quality factor of different antennas, the resistors change and according to this, the received input voltage will change as well. In commercial reader products the output power as well as the antenna structure and the quality factor are constant. That way the received voltage can be defined first, and the receive structure is adapted to that. In this evaluation reader it is possible to change the antenna, quality factor and output power, which results in a wide input voltage range. To reduce the complexity to handle this reader, the AGC was chosen as input structure.

For developing the AGC the bandwidth of the feedback loop has to be defined, to be able to be fast enough to follow the changes of the input voltage, if another antenna is connected, or the amplifier provides more energy. On the other hand, the gain regulation time constant has to be sufficiently slow to avoid to cancel the amplitude modulation, caused by the LM of the transponder. Two regulated amplifier stages are used, to avoid too much bandwidth variation associated with the gain control.

The principle of the AGC is depicted in Fig. 9. The

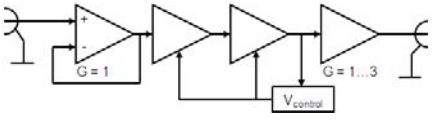

Figure 9. AGC block diagram

received signal from the antenna is connected to the SMA connector (2a). At the connector (2b) the output signal of the AGC can be observed, or it can also be used to connect any signal directly to the ADC. The AGC consists of a voltage follower, not to load the input, and is followed by two variable amplifiers. At the output of the second amplifier, the signal is observed and a feedback loop is implemented with two variable resistors which control the gain of the amplifiers. The AGC is dimensioned so that the output is always constant at 2.3 Vpp for an input range from 1 Vpp to 6 Vpp. To allow a higher input flexibility, additionally the input range can be shifted by the variable resistor (2c).

Furthermore if a higher output voltage is needed, if for example another ADC, or equipment is connected, it is possible to amplify the output to the desired voltage, by tuning the variable resistor (2d).

3) Supply unit PCB: Block 3 is used for the supply generation for the whole PCB. On board 24 V are needed for the power supply of the high voltage amplifiers as well as the current stage, and 12 V for the input amplifiers as well as the low pass filter and the AGC block.

The power supply is connected at (3a) and should be 24 V. A green control LED (3b) indicates the power supply. In case of wrong polarity LED (3c) is on, and the polarity of the supply voltage has to be changed.

The input voltage is stabilized by a set of capacitors, to filter any voltage ripple on the supply voltage. For the 12 V supply, the input voltage is regulated by a voltage regulator and stabilized again.

The connectors at (4c) are prepared to supply additional components such as a fan, if the reader is embedded in a housing.

4) Supply unit ML507 board: In addition to the board supply an extra supply unit is implemented to supply the ML507 board as well. This supply generation is prepared for a demonstration purpose, to reduce the number of external supply voltages. The voltage regulator is built similar to the supply unit for the PCB.

V. Characterization

To characterize the evaluation reader, different test scenarios were defined.

One important parameter is the output power of the transmit amplifier. To be able to define the output power, when the amplifier is loaded, a shunt resistor is connected to the amplifier with an SMA cable, and the signal at the resistor is measured. Using Eqn. 5 and the measured voltage (V_{pp}) at the resistor (R), the output power (P) of the evaluation reader can be calculated.

$$P = \frac{\left(\frac{V_{pp}}{2\sqrt{2}}\right)}{R}. \tag{5}$$

According to the measurement the output power can be varied from 120 mW to 2.1 W.

The highest field strength which can be achieved with this setup and the ISO/IEC 10373-6 PCD 1 Q 35 antenna is 6.6 A/m in 37.5 mm distance. This is less than the intended 7.5 A/m, but enough for a demonstration reader and first tests.

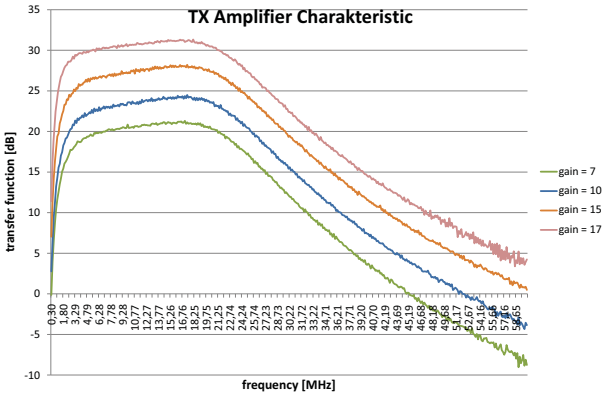

Figure 10. Transmit Amplifier characteristic

With a network analyzer and several attenuators, the transfer function of the amplifier at different gains was characterized and can be found in Fig. 10. The amplifier has a lower cut off frequency at 2 MHz, which is caused by the balun at the output. The amplifier has an almost linear characteristic between 2 MHz and 20 MHz, showing slightly increasing gain over the frequency. The upper cut off frequency can be found at 20 MHz. It can be seen that the output characteristic does not change significantly at different gains.

Measuring the noise figure (NF) according to Eqn. 6, the noise figure of the amplifier is 6 dB.

$$NF = SNR_{in,dB} - SNR_{out,dB} \tag{6}$$

The gain adjustment can be done by 2 variable resistors continuously.

The main parameter at the AGC is the output voltage range related to the input voltage range. To be able to define the behavior of the AGC, the dynamic range (DR) of the input and the output is defined. Eqn. 7 indicates the relation from the lowest to the highest voltage, and defines the DR of the input as well as output.

$$DR = \frac{V_{max}}{V_{min}} \tag{7}$$

For the measurement the AGC was connected to a frequency generator which provides a signal at carrier frequency and a voltage sweep. Fig. 11 shows the output voltage as function of the input voltage. It is shown that the output voltage has a linear gain for an input range from 1 Vpp to 6 Vpp. The output voltage increases from 1.8 Vpp to 2.5 Vpp. According to Eqn. 7, this means the output has a DR of $DR_{out} = 1.39$, compared to $DR_{in} = 6$ of the input.

VI. Conclusion

This paper shows the development of an evaluation reader, to be able to characterize and compare VHD concepts. The results give an idea of the impact of each scenario and are used for further development in contactless technologies.

The evaluation reader can be used, due its very flexible

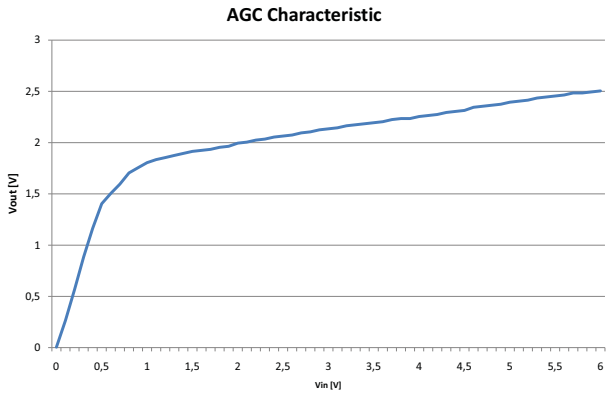

Figure 11. AGC output characteristic

design, as reader for various RFID based standards such as item level tagging (ISO/IEC 18000-3 [5]), vicinity labels (ISO/IEC 15693-2 [6]) and secure proximity smart cards (ISO/IEC 14443 [7]).

Measurements show the functionality and the dynamic range of the reader. With an on board power amplifier, which provides up to 2.1 W, the platform can be used as very flexible reader for demonstration and measurement purpose. Due to the reduced supply voltage, as described in the requirements, the goal to achieve full coverage of the ISO/IEC 10373-6 test standard couldn't be reached with these settings. Improvements are under development to further extend the coverage.

The actual setup requires two independent power supplies. One is needed to power the FPGA at 5 V, and a second one, with 24 V for the evaluation board. The additionally required 12 V on the evaluation board is generated by a linear voltage regulator which is not very efficient, but provides an output voltage with a very low ripple. For demonstration purpose, and to host the whole setup in a single and compact housing, further improvements are ongoing to built a single power supply. A transformer should provide all required voltage levels, which will be rectified and stabilized on board.

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