Minimizing intrinsic input leakage current and capacitance in hybrid sensor readout circuits

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Introduction

Noise in many sensor systems and particularly in radiation detection systems is determined by the input capacitance and leakage current [1]. In hybrid detection systems a protection against electrostatic discharge, ideally transparent, adds parasitics at the input pad. Sensors representing small equivalent capacitance seen from the input or small leakage (or both) are sensitive to such additional parasitics of the readout electronics [2]. This work focuses on reducing these parasitics. Focusing on hybrid sensor for ionizing radiation detection, the radiation tolerance has also been considered. Input protection pads targeting minimized increase in leakage current due to Total Ionizing Dose (TID) have been implemented in REDComET (Radiation and Electrostatic Discharge Combined Effects Test Chip) fabricated in 180 nm CMOS. In addition the testchip studies techniques for the input leakage current compensation: leakage current originating from the detector as well as from the pad protection.

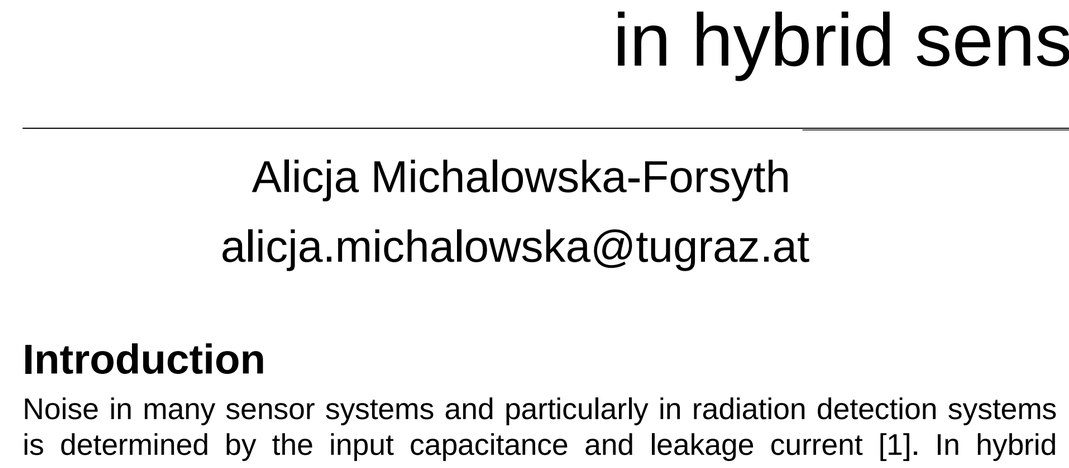


Fig. 1. Detector, readout circuit itself and its onchip ESD protection contribute to parasitic leakage current and capacitance, parasitics critical in low noise applications.

Test structures

Electrostatic discharge protection structures included on REDComET can be arranged in three categories [3]:

A) Diodes. Include linear and waffle layout. Since the on-current flows along the edges in case of the waffle layout conduction of the ESD current should be better, what is confirmed by TCAD simulations. On the other hand the extracted capacitance is lower for the linear diode, having lower side-wall capacitance. To find the best $C_{PARASITIC}/I_{ESD}$ ratio compromise, 10 structures of different layout and spacing will be measured.

Fig. 2 2D and 3D simulations with Sentaurus TCAD have been performed in order to determine the optimal layout of ESD diodes [3]

B) Single MOS structures cover primarily Gate Coupled NMOS (GCNMOS) with experiments on enclosed layout performance against ionizing radiation and negative gate bias in order to minimize the leakage current in normal operation.

C) Substrate Pump NMOS is investigated as more reliable way of triggering the bipolar action under transient event (ESD). Optimization in TCAD 2D was performed.

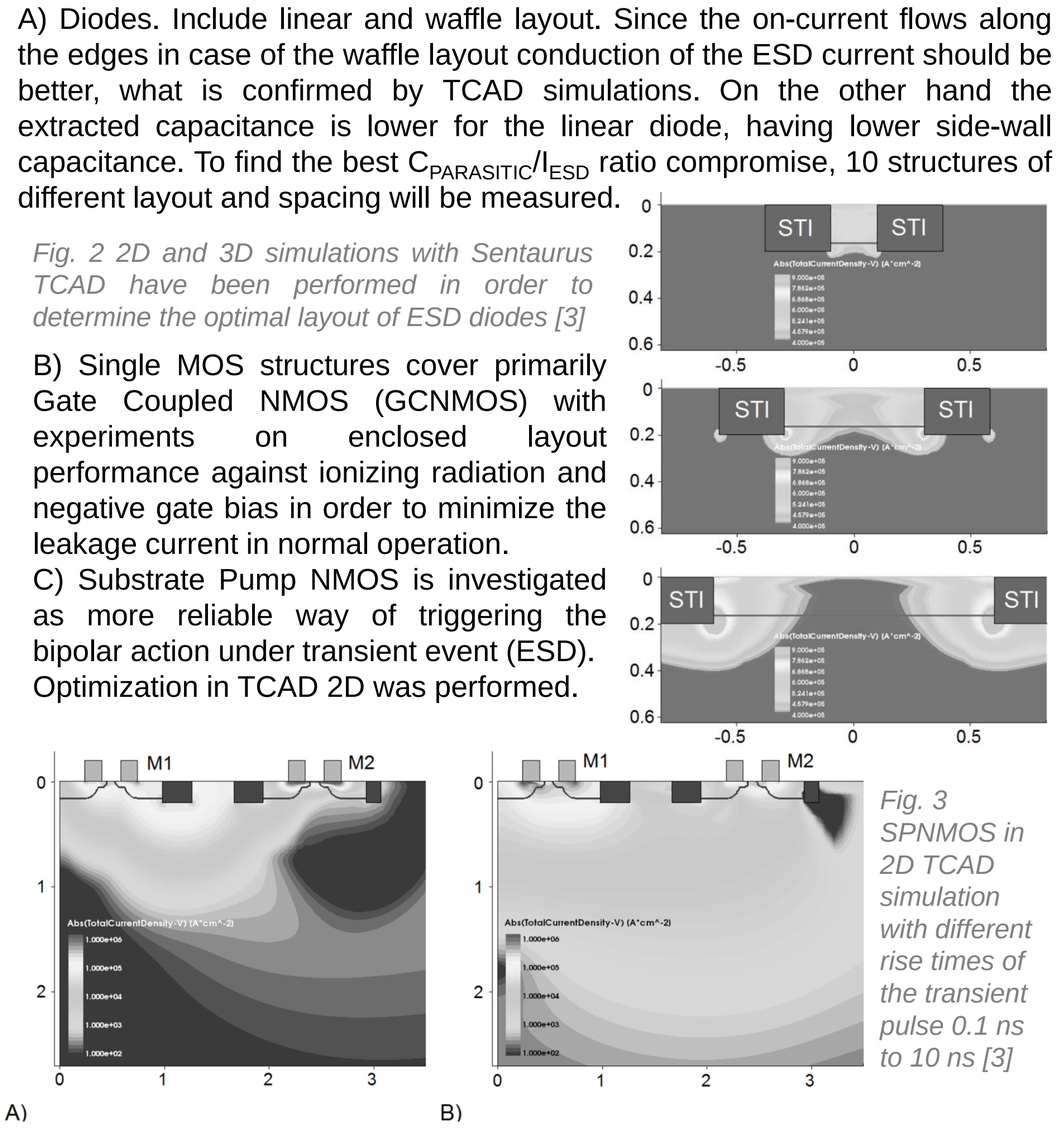


Fig. 3 SPNMOS in 2D TCAD simulation with different rise times of the transient pulse 0.1 ns to 10 ns [3]

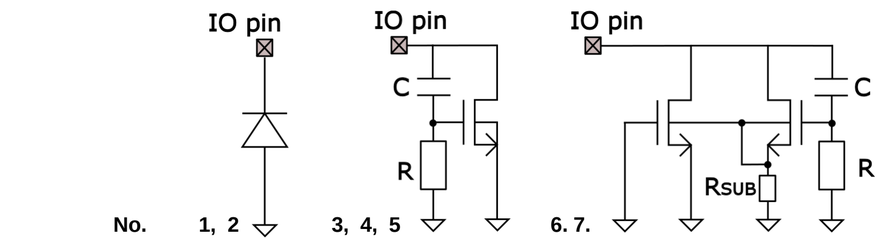


Fig. 4 Electrostatic discharge protection structures implemented REDComET: diodes (1-2), Gate-Coupled NMOS (3-5) and Substrate pump NMOS (6-7) [3]

Test chip

No	(*) Devices of comparable area	(**) Input capacitance	Expected ESD performance	Expected I_{LEAK} post-irradiation
1	Diode linear layout	1	+	–
2	Diode waffle layout	1.6	+ +	–
3	GCNMOS	2.2	+ + +	– – –
4	GCNMOS, ELT	-	+ + +	– –
5	GCNMOS, ELT, gate bias	-	+ + +	–
6	GGNMOS with substrate pump	2.4	+ + + +	– – –
7	GGNMOS with substrate pump, ELT	-	+ + + +	– –

Table 1. Main test structures on REDComET

(*) Constant n+ junction area for all devices
(**) C_{IN} from circuit simulation incl. extracted param. Unit is arbitrary with linear diode as reference.

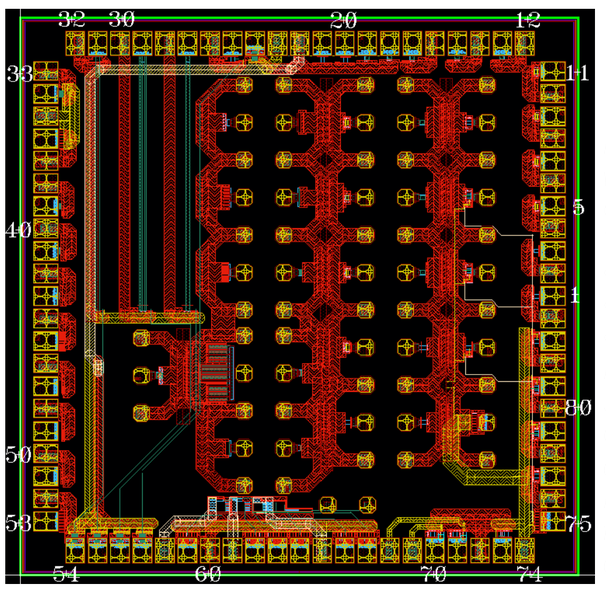


Fig. 5 REDComET, 180 nm CMOS, with multiple test structures for low $C_{PARASITIC}/I_{ESD}$ ratio
Target:
- *HBM > 2 kV,*
- *I_{LEAK}< 1 pA and C_{ESD}< 0.5 pF*
- *TID radiation tolerance*

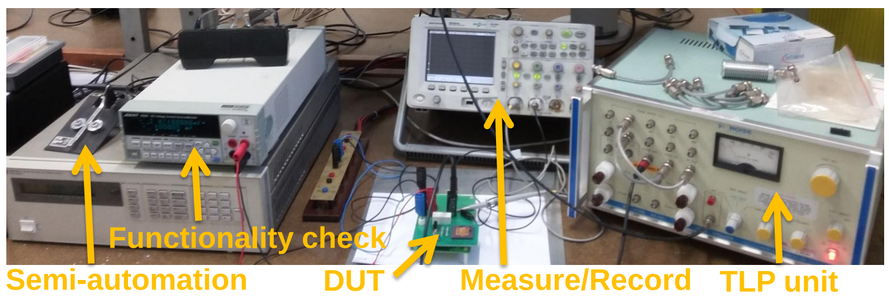
In the middle of the die: structures for S-parameter measurements with GSG probe to determine the capacitance vs. voltage and frequency.
In addition to simple protections further structures for leakage current compensation are implemented.

Test plan

On top of the capacitance and leakage current measurements, the following facilities are planned for performance determination of given test structures:

A) For ESD-like transient events tests a transmission line pulse (TLP) lab is available at the IFE/TU Graz with charge voltage of 40 V to 4.4 kV and pulse width of 50 ns .. 1 µs. Possibilities for HBM gun tests are being investigated.

Fig. 6 TLP lab to test ESD-like transient pulses with 50 ns to 1000 ns rise times



B) Total Ionizing Dose tests are planned with X-rays<200keV and TID<1Mrad.

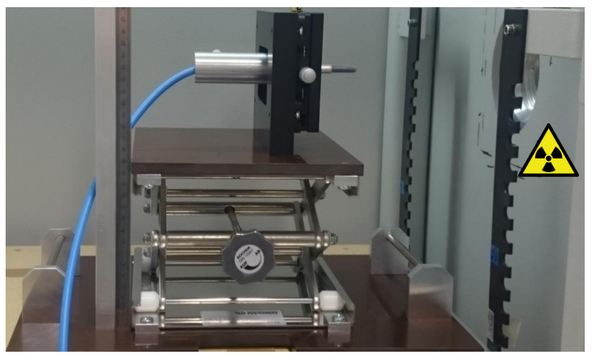


Fig. 7 Irradiator at MedAustron: XYLON X-ray tube 60 keV mean energy, TID adjustment from 0.4 to 300 rad/s, multiple TID calibration options

Summary

Measurements of the test structures implemented on REDComET testchip should determine the best compromise in terms of $C_{PARASITIC}/I_{ESD}$ ratio amongst structures of different types and layout. The main challenge is the necessity to perform multiple destructive tests on a limited number of samples.

Acknowledgements

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References

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[2] O. Gevin *et al.*, “Imaging X-ray detector front-end with high dynamic range: IDeF-X HD”, *NIMA*, vol.695, 2012

[3] A. Michalowska-Forsyth et al., “Design and theoretical comparison of input ESD devices in 180 nm CMOS with focus on low capacitance”, *e & i Elektrotechnik und Informationstechnik* 2018

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