Modular Test System Architecture for Device, Circuit and System Level Reliability Testing

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***Abstract*—Reliability stress testing of power semiconductors requires significant development effort for a test apparatus to provide the required functionality. This paper presents a modular test system architecture which focuses on flexibility, reusability and adaptability to future test requirements. Different types of tests for different devices in application circuit configuration can be implemented based on the same modular test system concept. Vital parameters of the device under test (DUT) can be acquired in situ during the running stress test. This enables to collect drift data of this parameters. The control and data acquisition parts of the test system are separated from the actual test circuit. With this physical separation, the same control part can be used for different types of tests. Experimental results of a prototype test system are provided.**

***Keywords*—aging, DC-to-DC converter, drift data, in situ measurement, life time, power semiconductors, reliability testing, stress conditions, test apparatus, wear-out.**

I. Introduction

A. Aim of work

Power semiconductors are exposed to thermo-mechanical stress during their functional use in application. The stress occurs due to power cycling of the device, which results in its aging, and eventually the device will fatigue and may fail. Therefore, reliability characterization of power semiconductor devices is of paramount importance during development of new devices [1]. To improve the reliability and operating safety of power electronic systems, knowledge about aging mechanisms and failure causes is crucial. Conducting life stress tests is necessary to provide results which can be compared to simulation data of device behavior in stress condition. This paper focuses on in situ life-cycle analysis and stress testing of DUTs in application circuit configuration. It presents a modular stress test system which is designed to meet several different test requirements and can be relatively easily adjusted to meet demands of such analyses in the future.

Most reports on reliability testing focus on the behavior of the DUT. Usually, the test systems are designed to analyze the wear-out of *one specific* device under certain stress conditions. This paper focuses on the design of the test system itself: A system is proposed (Fig. 1) that can be easily adapted to changing test requirements and DUTs such as discrete transistors, integrated circuits like a half-bridge configuration including driver, or a semiconductor power switch with additional built-in protection functions. A modular architecture is chosen for operating DUTs in a test setup equivalent to their real application circuit.

Figure 1: Prototype modular test system for active thermal cycling.

B. Novelty of the proposed modular test system

A well established test method consists in testing the bare DUT in a socket. This method has the advantage that characteristic device parameters, such as leakage current or transistor capacitances, can be well determined. Unfortunately, application-specific high load currents cannot be fed to the DUT when mounted in such a test socket.

Another conventional approach on the other side of production process is to submit the completely assembled field-application to a test. Here the whole system is put in an environmental chamber and tested in an exact application

configuration. The drawback to this method is that only little life-relevant data is gained as only few parameters can be monitored in such a configuration.

The modular test system described in this paper shows a solution in-between these two methods. As the devices are soldered on DUT boards, no device characteristic parameters can be measured which may be seen as a drawback to the proposed structure. In return, the devices can be committed to an application-equivalent high load condition. Through this condition drift data of voltages, currents, on-state resistance (R_{dson}) and device temperatures are acquired. This is the key novelty of this proposed new test system: gaining life time drift data out of an application-equivalent test setup.

The second advance compared to standard industry practice (e.g. HTOL [2]) is that it is possible to measure vital parameters of the DUT in situ during a running stress test. Thus, no interim measurements outside the test system are necessary.

The acquired life time data gained from various stress tests can be modeled by a Coffin-Manson approach which is covered in detail in [3].

This paper is organized as follows: Section I-C gives an overview on the status quo of other available test systems found in publications. In Section II the different types of stress tests are covered which can all be conducted with the modular test system proposed here. Section III describes the modular test system in detail and Section IV shows the first prototype implementation of such a system. Section V concludes this paper with a summary and an outlook to future work.

C. Discussion of state-of-art

There are several examples of existing test system implementations. All works cited in this paragraph focus on the device to be tested and the test system is designed to fit for this *one* purpose. Only the DUT and life test results of this DUT are focused on. The literature on these systems do not report on any attempt to use the available test hardware in a systematic way for different DUTs or types of tests, or both, as it is in the focus of the system proposed and discussed in this paper.

The authors of [4] introduce a test setup for high power IGBT modules with a common centralized test system architecture. The measured collector-emitter voltage V_{ce} of an IGBT transistor is cited to be the best indicator for the wear-out condition (bond-wire lift-off) of the DUT. The data acquisition during on-line stress testing will also be available by the modular stress test system proposed here. The implementation of the V_{ce} measurement circuit is described in detail in [5].

In [6], a test bench for IGBT modules similar to the one proposed in [4] is introduced. In addition to V_{ce} the junction temperature T_{j} is also monitored on-line. Again, this system has a centralized architecture which will make adaptations to future requirements quite difficult.

A test system for stress testing automotive smart power switches is proposed in [7]. It provides a high level of automation. A large number of devices can be submitted to stress in parallel. Three parameters (V_{ds}, I_{load}, R_{dson}) are acquired in situ during a stress test run for each DUT. A similar centralized architecture has also been used for the test system described in [8] in which the inductive clamping behavior of power MOSFETs after turn off is analyzed.

In [9] and [10] life stress test investigations of automotive smart power switches are presented. Both papers focus on the findings from the reliability stress investigations. Unfortunately little information on the test system is provided. The papers explain defects and failures on the DUTs, that occurred at the power semiconductors through repetitive short circuit operation.

II. Types of Stress Tests

Three common types of stress tests are discussed below. In all cases, the DUTs are placed in an environmental chamber for operation at elevated ambient temperatures. Interim device condition determination is performed during stress tests. Many reliability test systems do not support device condition determination, thus demanding regular user interaction. The proposed modular test system is designed to perform this condition determination in situ without user interaction. Moreover, the device condition can be acquired more frequently as the measurements are initiated automatically by the control software.

A. Active thermal cycling

This type of test either applies to discrete power transistors comprised in DC-DC topologies (such as buck, boost or Čuk converter) or to ASICs with integrated power transistors in a DC-DC topology, including their drivers. For operating life stress tests on solid state devices, the JEDEC 22-A108D standard [2] is available. The instructions for the High Temperature Forward Bias test (HTFB) [2] explicitly specify the necessary conditions for this type of test.

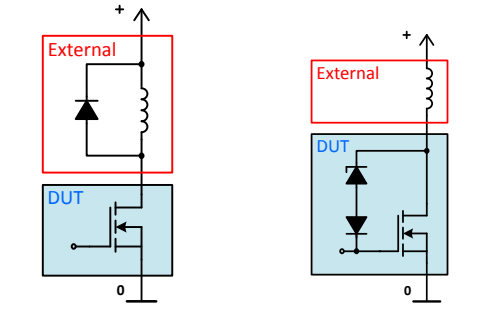
The stress test duration should reflect the time frame of the corresponding application. Therefore, the aging and thus the test time are accelerated by submitting the device to higher stresses than during nominal operation. The ambient temperature and self-heating of the power device are taken into account and the resulting junction temperature T_{j} is kept below or equal to the maximum specified operating temperature (typical values: $85\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ for consumer devices, $150\,^{\circ}\mathrm{C}$ for automotive devices). The bias input supply voltage is set to the maximum level specified for the DUT to still comply with the data sheet specification. The DUTs are connected to adjustable electronic loads outside the environmental chamber. The load is set to stress the DUTs at, or near the maximum rated current [2]. The DUTs are submitted to intermittent loads which toggle between high load of nearly $100\,\%$ until T_{j} reaches the maximum operating temperature and low load of $10\,\%$ until T_{j} reaches the ambient temperature. In practical reliability tests, the timing is chosen to reach the appropriate T_{j} temperature. This thermal toggling increases the stress on the DUT and accelerates its aging.

B. Automotive repetitive short circuit testing

This test is designed to stress smart power switches (SPSs), used in automotive applications. SPSs are equipped with

integrated driving, protection and diagnostic functions. In automotive applications they have taken the place of electromechanical relays for switching all kinds of electric loads, such as incandescent bulbs, solenoids and motors [11]. Protection against electric and thermal overload, a common feature of SPSs, is usually based on over-current detection and limitation, junction temperature sensing and protective shutdown, if electrical or thermal maximum ratings, or both, are exceeded [12].

Standard AEC-Q100-012 [13] defines the test procedures for repetitive short circuit characterization, including test circuit configuration, ambient temperature and impedances. Test equipment designed to perform stress on SPSs is proposed in [7], but it again has a centralized and less flexible architecture. The source and load side impedances are selectable by passive components (i.e. air coils and power resistors). These impedances emulate the cable harness in a car. The DUTs are turned on in short circuit condition. The SPS will limit the DUT's load current and eventually shut down when the DUT's junction temperature T_j reaches the temperature limit (typical value: 150 °C). The SPS is repeatedly put in short circuit until malfunction occurs and life time data is recorded. The proposed modular test system is able to perform these types of tests, as the application hardware modules are exchangeable.



(a) Single MOSFET switch with freewheeling diode.

(b) Single MOSFET switch with clamped gate.

Figure 2: Circuits for switching inductive loads.

C. Inductive load clamping

Integrated power switches for automotive applications must be capable of switching inductive loads, while employing a minimum of additional components. The common approach would be to use a freewheeling path as in Fig. 2(a) to demagnetize the inductance after transistor turn-off. In automotive applications the cost efficient solution is an integrated gate clamp, as shown in Fig. 2(b), which limits the drain-source voltage of the power MOSFET during turn-off. In fact the MOSFET turns on again until the load inductance is fully demagnetized. The main drawback is that the inductive energy which dissipates in the power switch during turn-off causes a significant rise in junction temperature, posing severe stress on the DUT.

Therefore, repetitive inductive clamping stress tests are of interest, too. In [8], a test system designed for such purpose is introduced which again has a centralized architecture. For the definition of stress conditions, passive inductive loads are replaced by active driving circuits which provide the DUTs with current pulses of arbitrary shape. These driving circuits emulate the triangular switch-off current ramp which an integrated power switch would see with a real inductive load. Also here, the DUTs are placed in an environmental chamber to submit them to the worst ambient temperatures to accelerate the ageing process. The proposed modular test system is able to perform these types of tests as well.

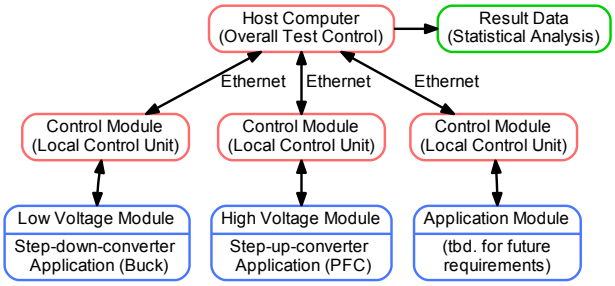


Figure 3: Test system architecture.

III. Modular Test System Design

The proposed modular test system architecture is shown in Fig. 3. The test control is split into two instances, namely the host computer and the control module. The host computer is *one* unit which controls the overall test flow and communicates with the control modules. It also controls external periphery, such as power supplies and electronic loads, and stores the measured data to the file system. The control modules may be *many* units (typically in multiples of 8) and are connected to the host computer via Ethernet network. The host computer forwards the stress pattern to the control modules and receives preprocessed (digitized and filtered) measurement data and status information. Each application module is connected to one control module which controls the application test, performs measurement data acquisition and logs device status information. This information is sent back to the host computer which stores the data. The application modules are tailored to individual types of test.

The essential advantage of this test system architecture is the separation of the control and data acquisition parts from the actual test circuit. With this architecture the same control and data acquisition parts can be used for different types of tests. Only the test circuits (blue boxes in Fig. 3) need to be redesigned. In the following, the test circuit will be referred to as application module.

A. Control module

The control module (Fig. 4) is the core control element for the test. It consists of the following circuit blocks:

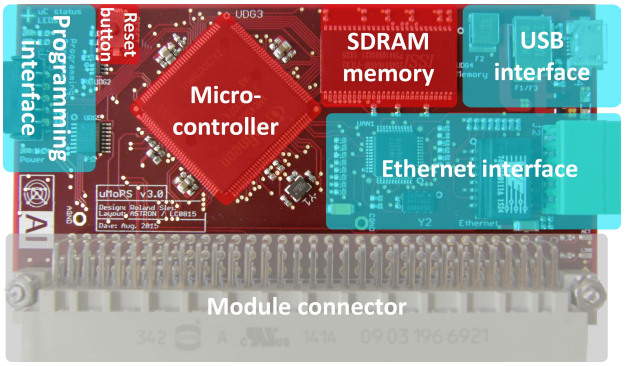


Figure 4: Control module.

- Infineon XMC4500 microcontroller [14].
- 8 MB SDRAM memory.
- 13 digital input / output channels.
- 2 SPI interfaces, 6 PWM output channels.
- 4 digital-to-analog converter channels.
- 8 differential and 12 single-ended analog-to-digital converter channels.
- Over-voltage protection on all signals on the module connector.
- Available interfaces: 100 Mbit Ethernet, USB, programming.

This module is plugged onto an application module and controls the running test sequence; on a synchronous boost converter application, it provides the PWM-signal via a driver circuit to the half-bridge switching transistors. It senses the output voltage and closes the control loop by a digitally implemented PI-controller. During the test, it collects the measured data which usually are input and output voltages and currents (V_{in}, V_{out}, I_{in}, I_{out}) of the converter as well as the case temperature T_{c}. All data are digitized on the control module and sent to the host computer via Ethernet network.

The major advantage of this concept is that the measurements are directly performed on the application module. No long and complicated sense wiring to a data logger outside of the environmental chamber is required. Altogether, 20 analog measurement channels are available on the control module. This ensures the expandability for future applications or extensions to existing ones. Only a small change in the script code is needed for logging further signals, provided the signal is routed to the control module.

On the control module the implemented differential operational amplifiers are provided with different input voltage dividers to offer several voltage ranges. For the whole system the voltage attenuation of analog measurements is implemented as a stacked concept. It is possible to directly use the provided input ranges implemented on the control module. Another possibility is (referring to Fig. 5) to change the series resistor values on the application board in order to adapt the input voltage range. With this stacked topology it is possible to flexibly adapt the input voltage range to the specific application where it is needed.

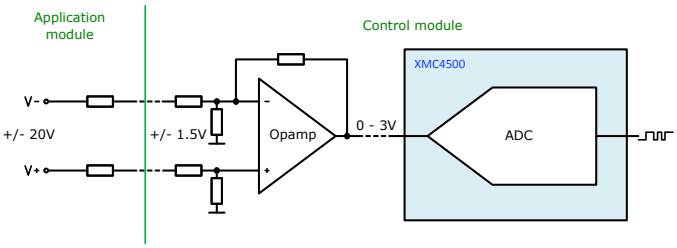


Figure 5: Analog measurement - stacked concept.

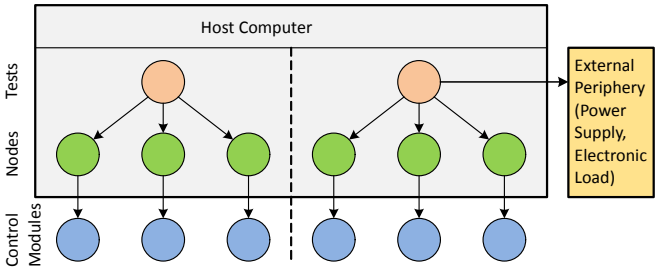


Figure 6: Software architecture: FSM control levels.

1) Software Architecture: The firmware implemented on the control module, together with a dedicated software environment on the host computer, allows an arbitrary stress pattern description. The test can be entered in the high level script language Lua [15] and no low-level microcontroller-specific code is needed for programming new test scenarios.

The software architecture, depicted in Fig. 6, follows a top-down approach. The test procedure on the host computer and the control modules is described by using multiple finite state machines (FSMs), in which each depicted circle represents a single FSM. The test procedure is described by the FSM-structure in which each single state can hold a chunk of Lua-code. A state transition can be triggered by internal or external events as well as by a special command invoked from the upper FSM.

The upper most circular, named test-FSM, controls the execution of multiple node-FSMs where each node subsequently controls a single control module FSM. Additionally, the test-FSM is capable of controlling external periphery, e.g. power supply or electronic load, to set voltage levels, current limits and cover automated power-up procedures. Based on this system approach, various test scenarios can be driven at the same time by simply modifying the Lua-script or FSM-structure, or both. A detailed description of the software architecture used with the proposed test system can be found in [16].

B. Application modules

An application module (blue boxes in Fig. 3) implements the main test circuit and is designed for one specific type of test. (E.g., for “active thermal cycling” the main test circuit may be a step-down or step-up converter.) Although they have different functions, some circuit blocks are common for all application modules. The most relevant ones are:

1) Guard block: An essential function for a stress test system is to ensure that the test setup is protected from catastrophic failure. When performing long-term tests on power semiconductors, the DUT may fail in short circuit. Under any circumstances the test system must be preserved in case of DUT damage. Preserving the DUT from further destruction immediately after failure also supports later physical analysis of failure root causes. The input current to the power circuit is monitored and an over-current limit is defined for each DUT. In case of short-circuit this limit is exceeded and the application module shuts down the power input immediately. This feature is implemented in hardware with a current sensor and an analog comparator to guarantee a fast response time (typical value: less than 2 µs). The failure event is then stored in an error latch and can only be reset by a test engineer intervention. Depending on the test circuit it may be necessary to monitor additional parameters. In this case a second parameter, such as the input voltage, is monitored which can trigger a power shut-down as well.

2) Device monitoring: All application modules incorporate voltage and current measurements (V_{in}, V_{out}, I_{in}, I_{out}) for input and output of the power circuit. Further voltage measurements can be analog status signals from the DUT and temperature signals (e.g., DUT case temperature T_{c}). Moreover, the control module provides several digital I/O channels to log digital status signals from the DUT or send digital stimuli to the DUT.

3) DUT board: In the modular stress test system the DUT is separated from the application module. This simplifies the task of replacing a failed DUT, while the application module can be reused. The DUT board is connected to the application module by a special connector, which may differ on various application boards. The type of this connector depends on the voltage and current ratings and the number of needed sense signals.

4) Module connector: As the control module is used on several application modules, all the application modules share the same type of connector [17].

5) Board identification: All application modules and DUT boards are equipped with a unique identity IC. This enables auto-detection of the connected boards by the control module.

6) Analog signal conditioning: As stated in Section III-A, operational amplifiers are provided on the control module to attenuate analog differential voltage signals to the single-ended voltage range of the analog-to-digital converters of the microcontroller. Additionally, all application modules have an analog signal conditioning block for performing further signal translations. E. g., a precision current source is implemented on an application module supporting high accuracy measurements of resistive temperature sensors. The voltage signal is amplified on the application module and then fed to the control module.

IV. Results

Exemplarily, the realization of the application module named "low voltage module" (Fig. 8) is discussed in the following:

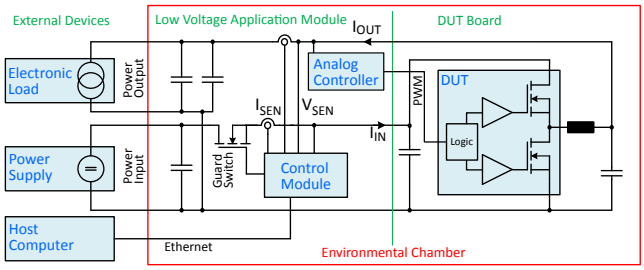


Figure 7: Low voltage module - simplified circuit.

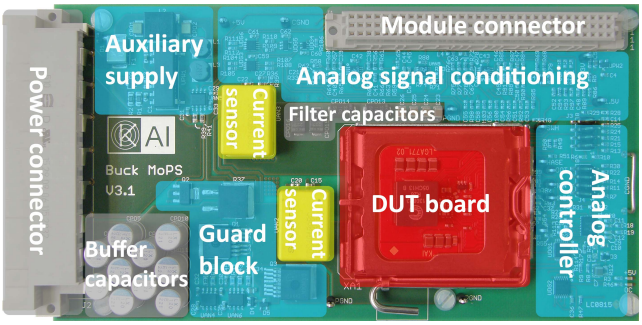


Figure 8: Low voltage application module and DUT board (red). DUT was removed for failure analysis.

A. Stress test example application

This application module submits the DUT to active thermal cycling. It comprises a step-down converter circuit designed for integrated power devices. The target device integrates two power MOSFET transistors in synchronous buck converter configuration, shown as the blue box "DUT" in Fig. 7. It has built-in gate drivers and sensing circuitry for current and temperature monitoring. It implements a temperature protection feature to shut down itself in improper operating conditions. It requires merely one PWM-signal input for operation. Interlocking and generation of correct turn-on signals for upper and lower transistor are generated internally.

The control loop of the DUT is closed by a dedicated analog controller from Linear Technologies [18]. This analog controller senses the output voltage and provides an appropriate PWM-signal to the DUT. In this case of application board, the connected control module operates only the test sequence and recording measurement data. The control loop of the step-down converter is closed by the aforementioned analog controller. The reason therefore is, that the converter runs at high switching frequencies (500 kHz to 2 MHz) and the microcontroller on the control module is not powerful enough to handle both the control loop and test sequence control, plus measurement data acquisition.

The DUT is available on a DUT board, shown in red in Fig. 8. To achieve an application-equivalent circuit behavior, the passive components (such as input and output capacitors and the filter inductor) must also be placed on the DUT board. This especially holds true for the input capacitance, as it influences the commutation loop inductance.

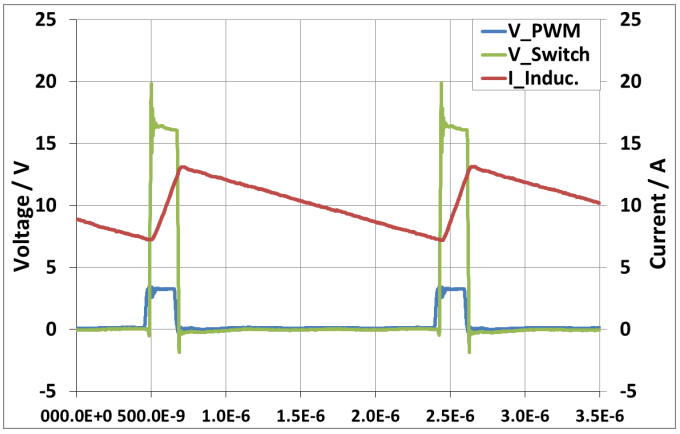
The application module holds the DUT board in a specialized socket with a high current carrying capability and low insertion impedances. It provides additional input and output capacitors (referred to as buffer and filter capacitors in Fig. 8) to support the power supply. It is equipped with two current transducers (yellow boxes in Fig. 8) for input and output current measurement. Conditioning for the logged current signals is achieved by operational amplifiers placed on the application module (block "analog signal conditioning" in Fig. 8) and fed directly to analog-to-digital converters of the control module. The operational amplifiers for the input and output voltage measurement are placed on the control module and by choosing the a reasonable series resistor, as shown in Fig. 5, the input voltage range is set. Signal conditioning for analog monitoring signals (T_{MON}, I_{MON}) implemented in the IC is done in a similar manner. For a case temperature measurement T_{c} the resistive temperature sensor is supplied from a constant current source and a voltage signal amplification is provided. The control module and the DUT board are plugged onto the application module and then placed in an environmental chamber. Fig. 10 shows all three boards plugged together. A guard block (Fig. 8) is likewise implemented on the application module, and will shut down in case of DUT failure.

The required connections to devices outside the chamber are:

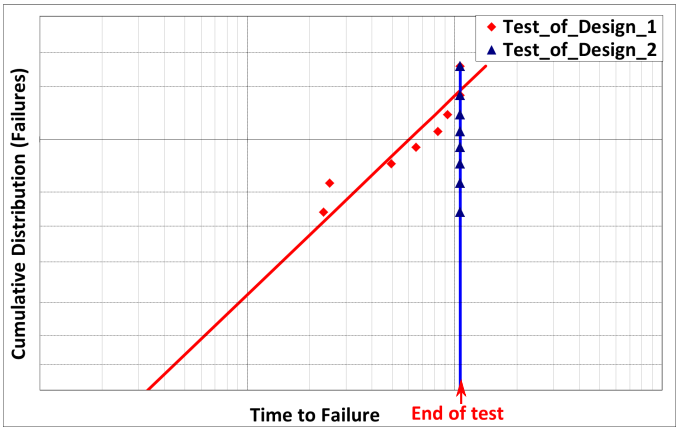
- Power input: connected to a high power supply.
- Load output: connected to an electronic multi-load for emulation of arbitrary load conditions.
- The control module is connected via Ethernet connection to the host computer.
- An auxiliary supply ($5\,\mathrm{V}$) for the application functions and the control module is necessary.

B. Test result data

A prototype test system with a low voltage application board in active thermal cycling configuration has been completed a year ago and has proven a valuable tool for chip development. The following results are gained from this system. Fig. 9(a) gives typical waveforms of the step-down converter application. The input voltage of $16\,\mathrm{V}$ is converted down to $1.5\,\mathrm{V}$ at an average load current of $10\,\mathrm{A}$. The figure shows the control PWM input signal, which is set to approximately $10\,\%$ duty cycle. Furthermore, the voltage at the switching node of the power transistors and the inductor current are given. Fig. 9(b) presents life time results of two stress tests. First, "Design 1" was tested and DUT failures where monitored. After that, the design of the DUT was improved and the same test was repeated. The test results of "Design 2" show that all DUTs now survive the stress test. The blue triangles of this test all lie in one line, because the stress test was stopped after reaching the full test time, at which time all DUTs were still operable. As with the proposed test system measurements are performed in situ during the running test, the exact failure times (diamonds and triangles) can be determined. Moreover, drift data of the voltages and currents as in Fig. 9(a) are continuously recorded and possible deviations are unveiled.



(a) Measured waveforms.



(b) Life time results.

Figure 9: Measurement results of life time tests conducted with prototype modular test system.

V. Conclusion and Outlook

A modular architecture for a fully automated stress test system has been presented. It can easily be adapted to future test requirements and different types of tests. The system is suitable for stressing a broad range of power transistors used in inverters. The test setup is built up as an application-equivalent circuit and can be designed for transistors of different voltage classes. Reliability tests for different power transistors can easily be realized, as the test circuit is clearly separated from the control and data acquisition part. Vital parameters of the DUTs are continuously logged during the running stress test. Drift data of voltages, currents and temperatures are collected to provide a base for subsequent statistical analysis. An example of a prototype test system realization for active thermal cycling was shown.

The next step is to develop a high voltage application module. This will incorporate a step-up converter circuit built up with wide band-gap transistors in the $500\,\mathrm{V}$ regime. The challenge with this module is that discrete transistors are used and the control loop, including interlock times, will be operated by microcontroller of the control module. Further development will focus on the modularization of circuit blocks at the level

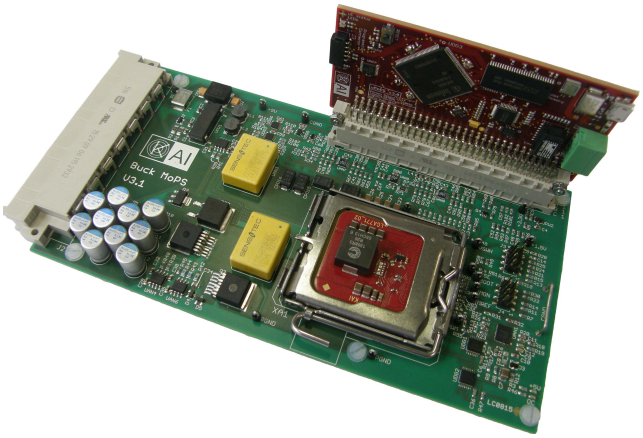


Figure 10: Low voltage application module, DUT board and control module plugged together.

of the application modules. This will reduce the development time of new test circuitry as readily designed circuit blocks are available for implementation.

VI. Acknowledgment

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