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Mismatch Reduction Techniques for Current-Mirror Based Potentiostats

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***Abstract*—Current-mirror based potentiostats suffer from systematic and random errors that mainly appear due to mismatch in the current-mirror. To limit the standard deviation of the error to less than 1.1 % over a dynamic range of four decades, either a high overdrive voltage or comparable big transistor dimensions are required. In this work, an optimized design approach for the current-mirror is presented. Based on the given accuracy and dynamic range requirements, an optimized programmable current-mirror is implemented. An accuracy driven design approach is used to achieve the required accuracy over the wide range of sensor currents, while keeping the area consumption low. Compared to a linearly scaled current-mirror based potentiostat design, an output stage area reduction by a factor of four is achieved. Additionally, the voltage headroom consumption is kept at a minimum. The potentiostat is implemented in a 130 nm CMOS technology and consumes an area of only 0.14 mm^2. The simulation results show that even in the worst case the specified accuracy is achieved over the complete dynamic range of sensor currents from nA to mA.**

***Index Terms*—Point-of-care (PoC) diagnostics, potentiostat, current-mirror, dynamic element matching, wide dynamic range**

I. Introduction

Point-of-care (PoC) diagnostics for biomedical applications have received increasing attention in recent years. The continuously rising technological connectivity among the population suggests to replace traditional optical PoC diagnostics by ones that are based on electrochemical readout principles. These electrochemical diagnose platforms promise to provide highly-accurate and fast results in non-laboratory environments, while keeping the medical costs at a minimum [1].

Diagnostics that are based on electrochemical detection mostly use amperometric measurement methods to extract information from the biosensor. These methods capture the current that results from a redox reaction at the sensor electrodes [2]. Amperometric measurement principles are usually carried out by three-electrode potentiostats. A potentiostat is a sensor front-end circuit, which maintains a desired potential difference between the working electrode (WE) and the reference electrode (RE) by adjusting the counter electrode (CE) according to the current that arises due to the electrochemical reaction [2].

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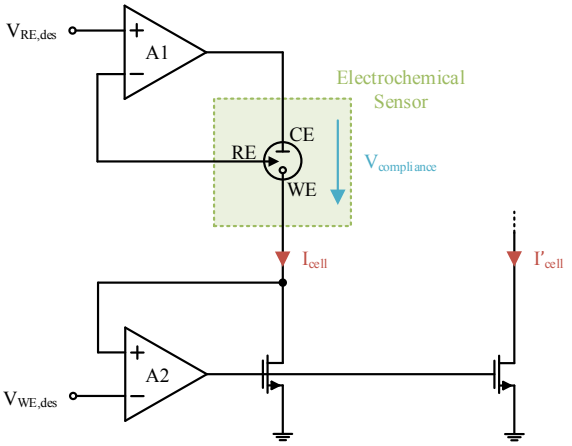

Fig. 1. Conceptual schematic of a current-mirror based potentiostat. The voltages $V_{RE,des}$ and $V_{WE,des}$ are used to drive the sensor. The resulting current is measured.

There are several topologies of potentiostats available, among which the amplifier that drives the WE and extracts the information of the biosensor is of special design interest. Topologies consisting of transimpedance amplifier (TIA) based designs [3], [4], current-conveyor based designs [5]–[8], and current-mirror based designs [9]–[11] were recently presented. TIA based designs and current-conveyor based designs suffer from a high voltage headroom requirement, thereby limiting the possible compliance voltage range for the sensor. The current-mirror based approach on the other hand, as shown in Fig. 1, just requires one transistor saturation voltage for proper operation. This makes this topology especially interesting for low voltage applications.

The advantage of the low voltage headroom requirement of current-mirror based designs comes at the expense of an additional error source due to the current-mirror. The systematic and random errors in the circuit lead to gain, offset and linearity errors in the sensor front-end. Conceivable ways to minimize these undesired effects are to increase the overdrive voltage of the current-mirror or to increase the active area of the corresponding transistors. Both of these possible countermeasures have their drawbacks. The former approach restricts the compliance voltage range, whereas the latter approach leads to a big area consumption, especially when designing for a wide dynamic range of sensor currents. In this work,

an optimized implementation is shown, which achieves high accuracy over a wide range of sensor currents, while the area and voltage headroom consumption is kept at a minimum.

The paper is structured in the following way. Section II describes the fundamental design considerations for the current-mirror based potentiostat. In Section III, the optimized design approach of the current-mirror is described and a comparison to a linearly scaled design is given. Section IV shows the achieved performance of the implementation. Finally, Section V concludes the paper by summarizing the main findings of the research work.

II. System Architecture of the Current-Mirror Based Potentiostat

In a current-mirror based potentiostat, the voltage across the electrochemical sensor is set by two operational amplifiers that are operated in a feedback-configuration, as shown in Fig. 1. The sensor current, which flows through the NMOS transistor controlled by amplifier $A2$, is replicated by a current-mirror structure. This replica can then be processed in the additional branch without any influence on the available compliance voltage range of the potentiostat.

However, adding a current-mirror adds an additional potential error source to the sensor interface. To minimize the systematic and random errors in the current-mirror, optimizations of the current-mirror based potentiostat were implemented. These optimizations include the use of a regulated-cascode, the implementation of an area-optimized programmable current-mirror and the use of dynamic element matching (DEM). A simplified schematic of the implemented topology is shown in Fig. 2.

The regulated-cascode keeps the difference between the drain-source voltages of the current-mirror transistors low and reduces errors related to the finite output impedance of the transistors. A symmetrical OTA with a PMOS input pair is used to perform this task. The choice of a PMOS input pair allows the potentiostat to use WE potentials close to ground. Thus, the addition of the regulated-cascode has no influence on the compliance voltage range of the topology.

To achieve a wide dynamic range in the sensor front-end, a programmable current-mirror was implemented. A 2-bit adjustable current-mirror for current down-scaling is used to process sensor currents up to the mA range. Using scaling factors of 1, 10, 100, and 1 000, a down-scaling of the sensor current to a range of 0 to 1 µA is possible. The down-scaling minimizes the power consumption of the front-end and reduces the constraints for the post-processing circuity, i.e. the analog-to-digital converter (ADC). An ADC with a fixed input full-scale range is then used to process the sensor current information. Depending on the result of the analog-to-digital conversion, the programmable current-mirror is adjusted to achieve optimum performance.

However, the area consumption of a high scaling factor current-mirror strongly depends on the required mirror accuracy. In the particular application of amperometric

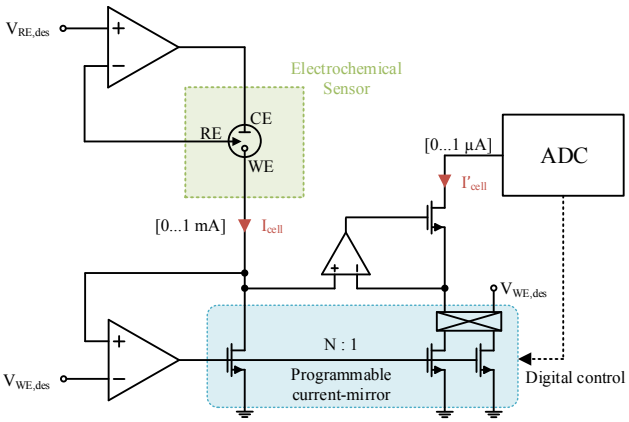

Fig. 2. Simplified schematic of the implemented current-mirror based potentiostat. A regulated-cascode is used to minimize the systematic error due to channel-length modulation. An area-optimized programmable current-mirror is used to achieve high accuracy over a wide dynamic range. Dynamic element matching on the mirror transistor side is used to further reduce the area consumption of the high current scaling current-mirrors.

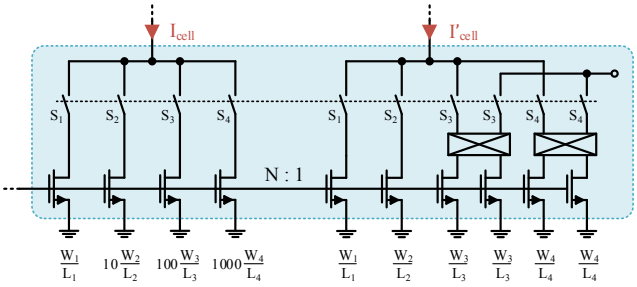

Fig. 3. Conceptual schematic of the programmable current-mirror. Different reference transistor dimensions enable a ratio dependent optimization.

measurements, a high processing accuracy is especially required for the lower current region. Thus, current-mirror scaling by adding additional parallel unit transistor elements on the input side soon leads to a considerable silicon area consumption. The respective optimum depends on the mirror scaling factor, therefore a programmable current-mirror was used to enable a ratio dependent optimization. In this optimized design, the four selectable regions of the current-mirror differ not only by the number of parallel input transistors, they are also different in terms of reference transistor dimension. This is illustrated in Fig. 3. The additional use of DEM results in a further reduction in area. A more detailed description of the realized optimizations in the current-mirror and the thereby achieved improvements are given in Section III.

III. Programmable Current-Mirror Design

Systematic errors are minimized by the use of a regulated-cascode structure. Random errors require proper transistor sizing. Using dynamic techniques area consumption can be reduced. The theoretical background of the design approach and the advantages compared to a linearly scaled design are given in the first part of this section. Based on the findings, the implementation of the optimized

current-mirror potentiostat is presented in the second part of the section.

A. Analytical Description of the Design Approach

The transistor is described using the square-law model [12]. The current factor is abbreviated by β ($= \mu C_{ox} W/L$, where μ is the channel mobility, C_{ox} the gate-oxide capacitance per unit area, W and L the transistor width and length).

While the influence of β mismatch in a current-mirror can only be addressed by increasing the transistor dimensions, threshold voltage mismatch can also be reduced by using a high overdrive voltage for the current-mirror transistors [13]. Assuming an optimal layout implementation and equal drain-source voltages at the transistors, the standard deviation of the input-referred relative current mismatch of a current-mirror, $\sigma(I_{err})/I_{cell}$, operated in saturation region, is found to be

$$\frac{\sigma(I_{err})}{I_{cell}} = \sqrt{\frac{{A_K}^2}{W\,L} + \frac{2}{(V_{gs}-V_{th})^2}\frac{{A_{V_T}}^2}{W\,L}} \cdot \sqrt{\frac{N+1}{N}}, \tag{1}$$

using variance propagation [13]. In (1), I_{err} is the input-referred current mismatch of a current-mirror with an input current of I_{cell} and a scaling factor of N. Furthermore, $V_{gs}-V_{th}$ is the overdrive voltage of the current-mirror, A_K and A_{V_T} the β and threshold voltage mismatch parameter of the transistors, and W and L the reference transistor width and length. As observable in (1), an increasing scaling factor N leads to a decreasing value of the term $\sqrt{(N+1)/N}$, which soon approaches a value of 1 for increasing mirror factors. Compared to a 1:1 current-mirror, a linearly scaled sizing with parallel unit transistor elements thus leads to an accuracy improvement by a factor of $\sqrt{2}$ for $N \gg 1$.

Without taking advantage of the increased accuracy, the area consumption of the current-mirror would scale by N. However, considering this property, a lower area requirement is obtained. In this area-optimized design with regard to a certain accuracy requirement, the left side of (1) is kept constant, and the required reference transistor area depending on the current scaling factor N is determined. The corresponding reordering of (1) leads to

$$W\,L = \left({A_K}^2 + \frac{2}{(V_{gs}-V_{th})^2}\cdot {A_{V_T}}^2\right) \cdot \frac{N+1}{N} \cdot \left(\frac{I_{cell}}{\sigma(I_{err})}\right)^2. \tag{2}$$

For increasing current scaling factors, the reference transistor area decreases in this design approach. Because of the term $(N+1)/N$ in (2), high scaling factor current-mirrors require a reference transistor area that is just half of the area of a low current scaling factor mirror. In other words, only the reference transistor is responsible for the inaccuracy of the current processing at high scaling factors.

Figs. 4 to 6 visualize the relationship between current-mirror accuracy and required active transistor area as a function of the current-mirror scaling factor. In these plots, the dashed trace shows the relationships for the linear current-mirror sizing, whereas the dotted trace shows the relationships for the proposed ratio dependent sizing. The visualizations are based on the analytical descriptions (1) and (2). As observable in Fig. 6, the biggest area saving due to the ratio dependent optimization is achieved in the high current scaling region. A current-mirror area reduction by a factor of 2 is obtained.

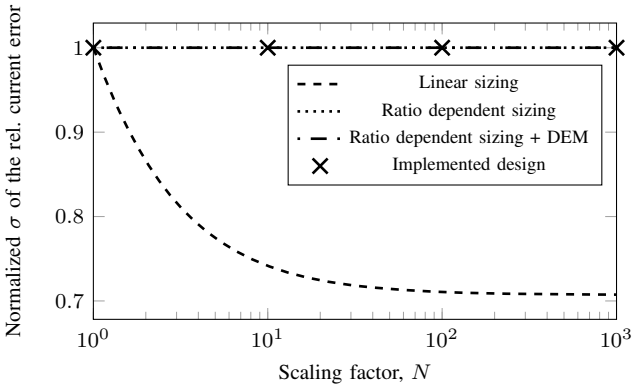

Fig. 4. Standard deviation of the relative current error depending on the current-mirror scaling factor for the different design approaches. Normalized plot to the standard deviation of a 1:1 current-mirror.

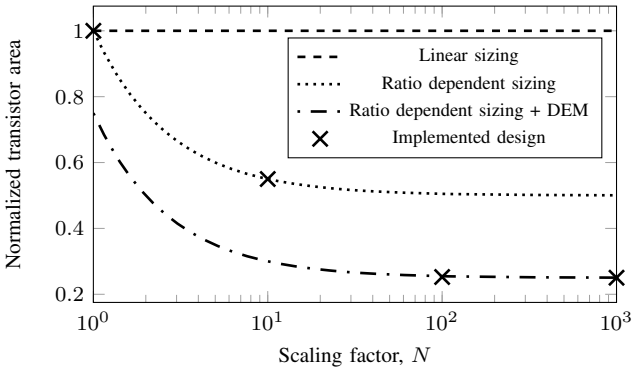

Fig. 5. Reference transistor area depending on the current-mirror scaling factor for the different design approaches. Normalized plot to the reference transistor area of a 1:1 current-mirror.

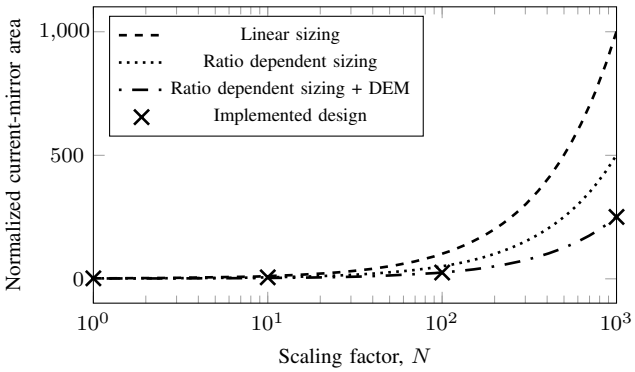

Fig. 6. Total current-mirror area consumption depending on the current-mirror scaling factor for the different design approaches. Normalized plot to the area consumption of a 1:1 current-mirror.

However, the area consumption of the high scaling factor current-mirrors is still dominating the overall area consumption. To address this problem, an additional optimization using DEM techniques was done in the circuit level implementation of the current-mirror.

B. Implementation of the Design Approach

As discussed in Section II, the wide dynamic range in the sensor front-end is reached by using a programmable current-mirror. One of the design limitations of the current-mirror would be flicker noise, which can be reduced by increasing the size of the transistors. To limit the current error to less than $1.1\,\%$ and the overdrive voltage to $200\,\mathrm{mV}$, a minimum transistor area of $80\,\mu\mathrm{m}^2$ with a W/L ratio of 0.2 was determined by simulation for the 1:1 current-mirror. Hence, the area of the transistors is already sufficiently high to keep the flicker noise at an acceptable level. According to the optimized design approach shown above, current-mirror areas of $160\,\mu\mathrm{m}^2$, $484\,\mu\mathrm{m}^2$, $4\,080\,\mu\mathrm{m}^2$, and $40\,080\,\mu\mathrm{m}^2$ result for the scaling factors 1, 10, 100, and 1 000, respectively. Apparently, the main area is consumed by the current-mirrors with scaling factors of 100 and 1 000.

To further optimize the implementation with regard to area consumption, DEM techniques were applied. As pointed out earlier, for the high scaling factors only the reference device transistor on the mirror side has a significant contribution to the current mismatch. Therefore, a dynamic switching between two reference transistors on the mirror side was implemented to increase the accuracy, as shown in Fig. 2. Using DEM only on the mirror side has the additional advantage of keeping the electrode connection away from a potential influence due to high-frequency switching, which is essential to perform accurate electrochemical analyses. The improvement due to DEM allows a further reduction of the transistor areas by a factor of up to 2, while achieving a similar accuracy in the current-mirror as without DEM. This is illustrated by dash-dotted traces in Figs. 4 to 6. Again, the biggest area savings are achieved in the high current regions. For this particular design, this leads to an active area reduction to roughly $2\,080\,\mu\mathrm{m}^2$ and $20\,080\,\mu\mathrm{m}^2$ for the current-mirrors with scaling factors of 100 and 1 000, respectively.

The relationship between accuracy and area consumption of the finally implemented design approach is additionally visualized by crosses in Figs. 4 to 6. Since the area consumption of the current-mirrors with scaling factors of 1 and 10 is comparable low, they have been implemented without DEM. The overall advantage in area consumption compared to a current-mirror design with linearly sized transistors is apparent. With focus on the application of low-cost PoC diagnostics, this results in significant cost savings in the production of the electrochemical read-out device.

IV. Potentiostat Performance Evaluation

The current processing accuracy of the implemented sensor front-end was characterized by Monte Carlo analysis. In this analysis, local as well as global process and mismatch parameter variation were taken into account. Depending on the sensor current, the appropriate range was selected.

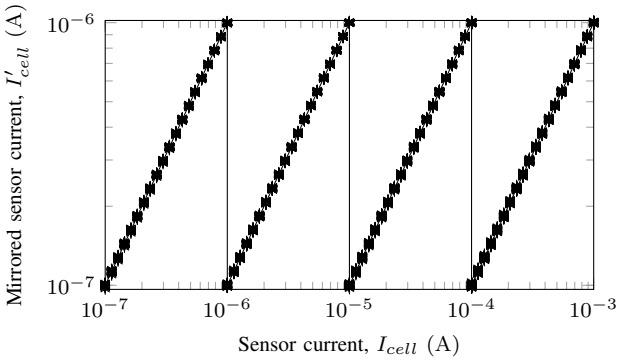

Fig. 7. Transfer characteristic of the implemented current-mirror based potentiostat. The solid line shows the nominal simulation run, whereas the stars show the result of the Monte Carlo simulation.

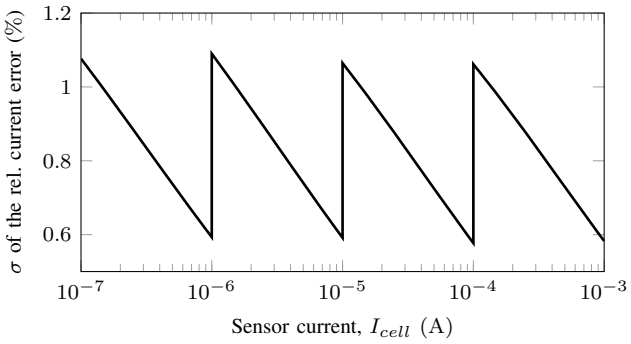

Fig. 8. Standard deviation of the relative current error of the implemented current-mirror based potentiostat.

Fig. 7 shows the resulting transfer characteristic of the current-mirror based potentiostat. The four regions of the programmable current-mirror and the corresponding scaling of the sensor current are clearly observable. The standard deviation of the relative current error depending on the sensor current is shown in Fig. 8. As can be seen, the current error in each region of the programmable current-mirror decreases with increasing sensor current. This is due to a rising overdrive voltage in the current-mirror for higher currents. The standard deviation of the worst-case current error is less than $1.1\,\%$ over the complete dynamic range of sensor currents. This allows the current-mirror potentiostat to accurately distinguish between biochemical parameters in the application of amperometric measurements.

The circuit was realized in a 130 nm standard CMOS process as a main building block of a wirelessly-operated electrochemical measurement platform IC. Fig. 9 shows a layout picture of a test-chip that is currently in production. The chip contains a slightly modified version of the presented current-mirror based potentiostat. Compared to the discussed implementation, the area of the high scaling factor output stage is reduced due to an application related requirement, leading to a standard deviation of the worst-

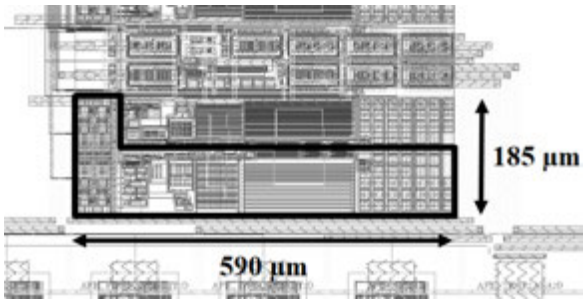

Fig. 9. Part of the test-chip layout containing the current-mirror based potentiostat.

case error of roughly $2.2\,\%$ in this region. Taking the additional area consumption of this stage into account, the total area of the presented implementation can be estimated to a value of less than $0.14\,\mathrm{mm}^2$.

V. Conclusion

Accuracy and area consumption trade-offs in current-mirror based potentiostats were presented. A design methodology for the current-mirror optimization using a reconfigurable topology was proposed. The accuracy driven design approach leads to a reduction in the area consumption of wide dynamic range current-mirrors due to a mismatch-optimized transistor sizing. Analytically derived design rules were verified by simulation in a 130 nm CMOS technology. The achieved accuracy over the complete dynamic range proves that the interface is suitable for amperometric measurement methods. The low area consumption and the high compliance voltage range of the design makes it a potential candidate for low-cost PoC diagnostics in biomedical applications.

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