KASLR: Break It, Fix It, Repeat

C. Canella (@cc0x1f), M. Schwarz, M. Haubenwallner, M. Schwarzl, D. Gruss

ACM AsiaCCS 2020

Graz University of Technology

- Meltdown requires hardware mitigations

Motivation

- Meltdown requires hardware mitigations
- How do these mitigations work?

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- How do these mitigations work?
- Microarchitectural KASLR breaks are fast and reliable

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- Meltdown requires hardware mitigations
- How do these mitigations work?
- Microarchitectural KASLR breaks are fast and reliable → how do we prevent them?

- CPU uses data in out-of-order execution before permission check

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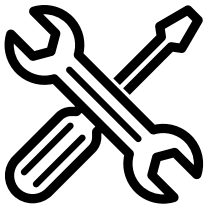
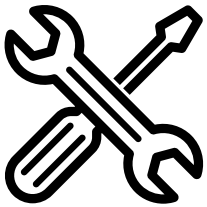
→ Read arbitrary memory



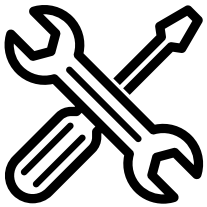
Assumptions

1. Stalling CPU might be too costly



Assumptions

1. Stalling CPU might be too costly
2. Stalling might require redesigning parts of CPU pipeline



Assumptions

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Hypothesis

Load is executed, returned value is zeroed out

Verifying the Hypothesis

Two tests:

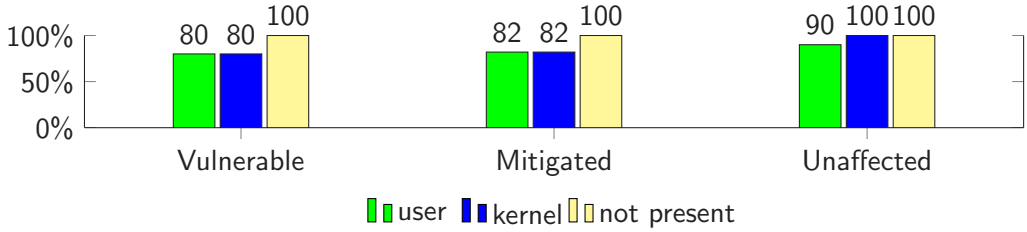
1. Perform Meltdown attack

Verifying the Hypothesis

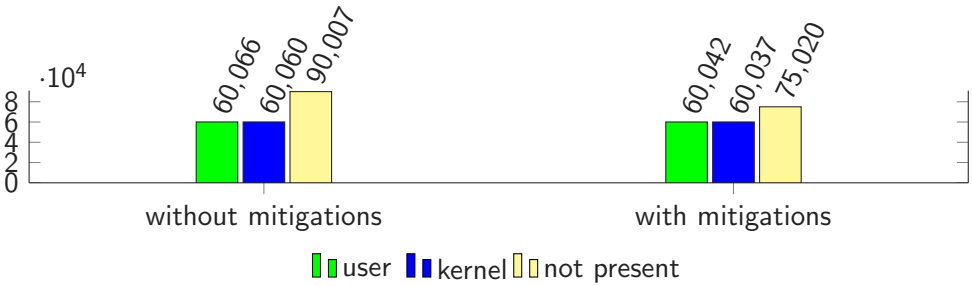
Two tests:

1. Perform Meltdown attack
2. Use Performance Counters

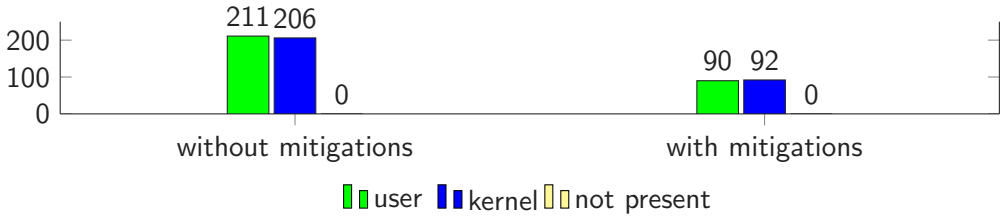
- Intel: CYCLE_ACTIVITY.STALLS_MEM_ANY
- AMD: Dispatch Stalls

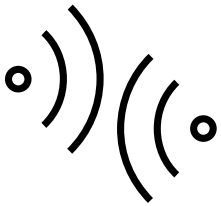


- Track number of issued μOPs on the load ports
- UOPS_DISPATCHED_PORT.PORT_2, UOPS_DISPATCHED_PORT.PORT_3

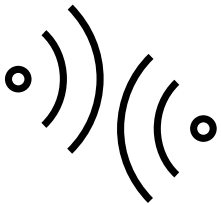


- L1D_PEND_MISS.PENDING_CYCLES

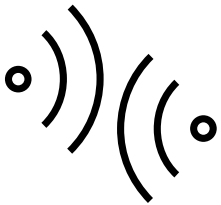




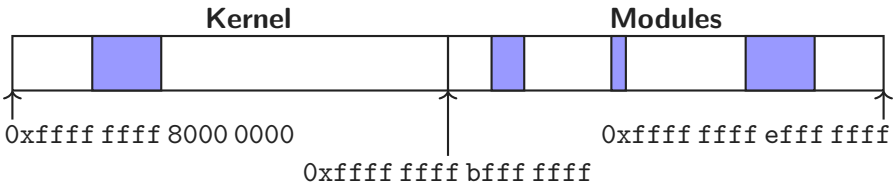
- Can we use the hardware-based mitigations for an attack?

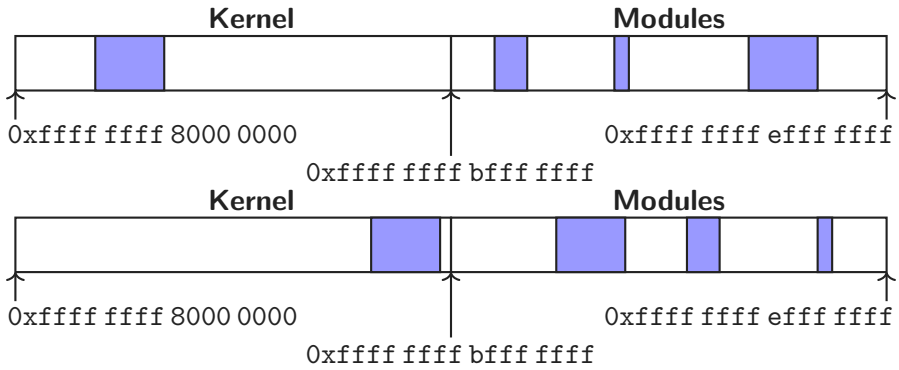


- Can we use the hardware-based mitigations for an attack?
- EchoLoad: fast and reliable KASLR break



- Can we use the hardware-based mitigations for an attack?
- EchoLoad: fast and reliable KASLR break
- Encodes the returned value in the cache


Kernel
Modules
0xffff ffff 8000 0000
0xffff ffff bfff ffff
0xffff ffff efff ffff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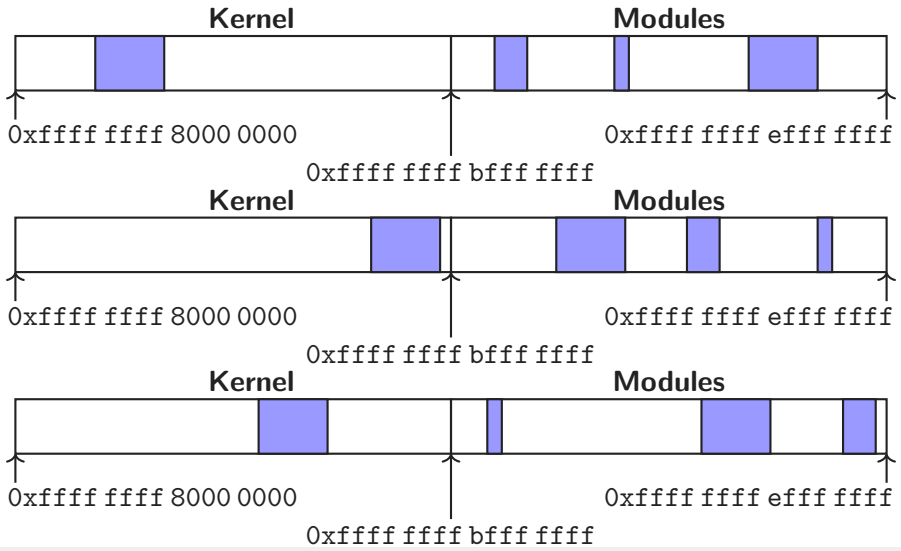
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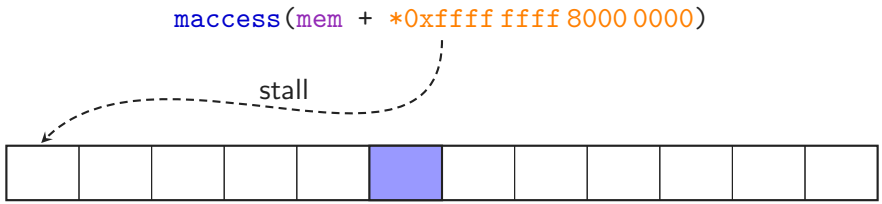
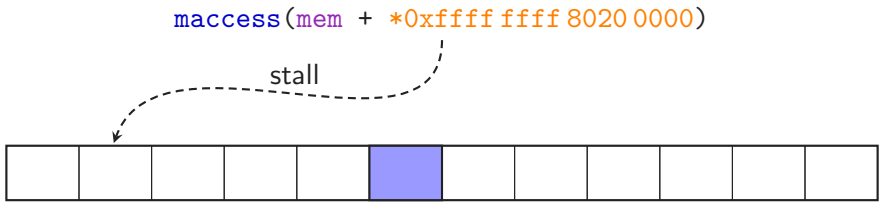
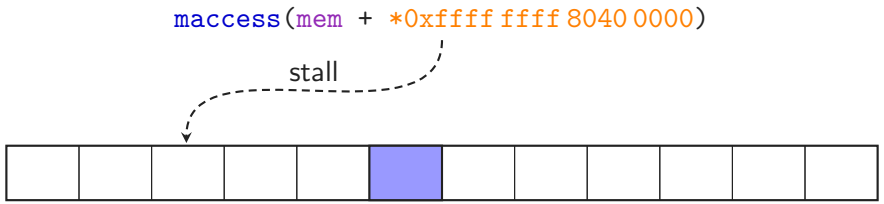
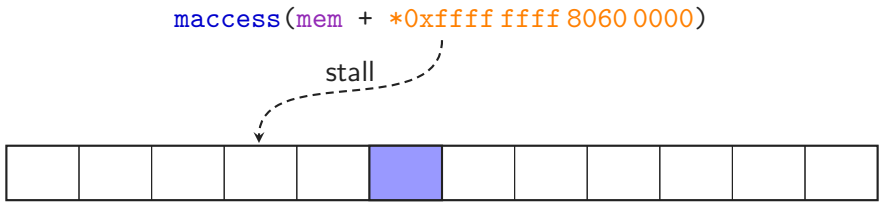
0xffff ffff efff ffff
0xffff ffff bfff ffff

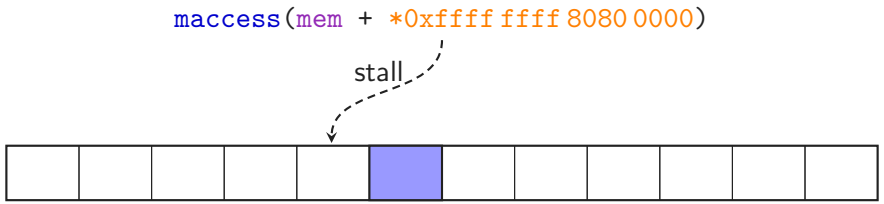
```
maccess(mem + *0xffff ffff 8000 0000)
```

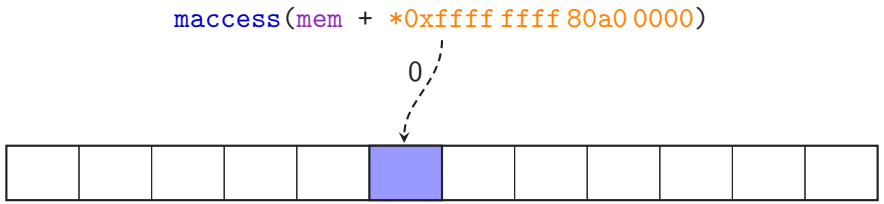

maccess(mem + *0xffff ffff 8000 0000)
stall


maccess(mem + *0xffff ffff 8020 0000)
stall


maccess(mem + *0xffff ffff 8040 0000)
stall


maccess(mem + *0xffff ffff 8060 0000)
stall


maccess(mem + *0xffff ffff 8080 0000)
stall


maccess(mem + *0xffff ffff 80a0 0000)
0

CPU		Speculation		TSX		Segfault	
i7-6700K	Time (F-Score)	63 µs	(0.999)	48 µs	(1.000)	133 µs	(1.000)
i9-9900K	Time (F-Score)	33 µs	(1.000)	29 µs	(1.000)	86 µs	(1.000)
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- Works in SGX and JavaScript
- Enables Meltdown from JavaScript on unpatched x86

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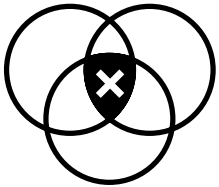
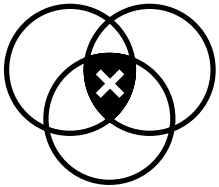
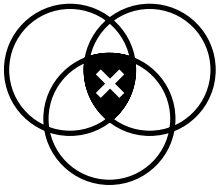


Timing difference



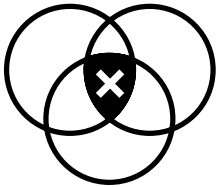
Timing difference

- between mapped and unmapped pages



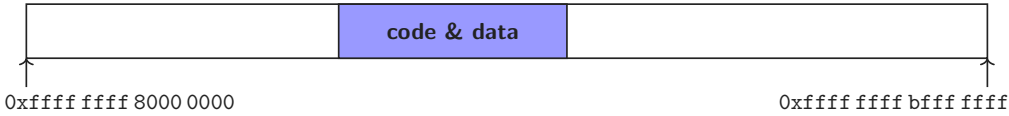
Timing difference

- between mapped and unmapped pages
- for different page sizes

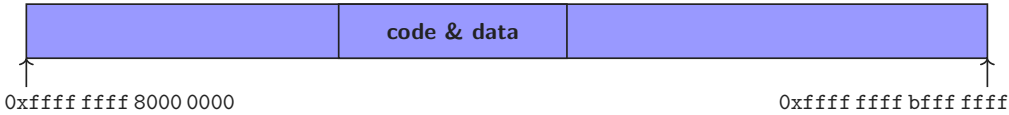


Timing difference

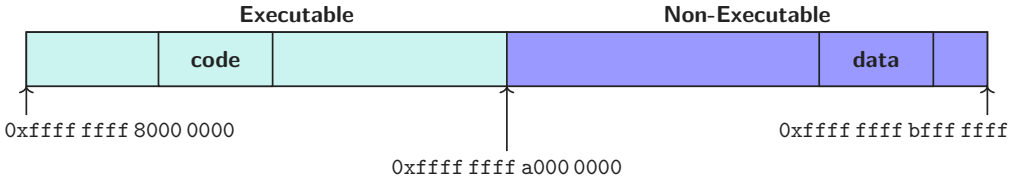
- between mapped and unmapped pages
- for different page sizes
- between executable and non-executable pages



Current Linux design



Step 1: Mitigating difference between mapped and unmapped pages



Step 2: Mitigating difference between executable and non-executable pages

```
maccess(mem + *0xffff ffff a000 0000)
```

```
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```

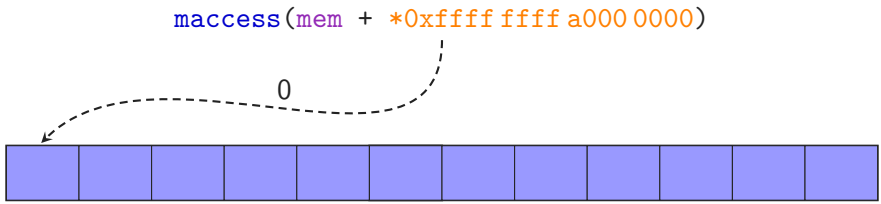
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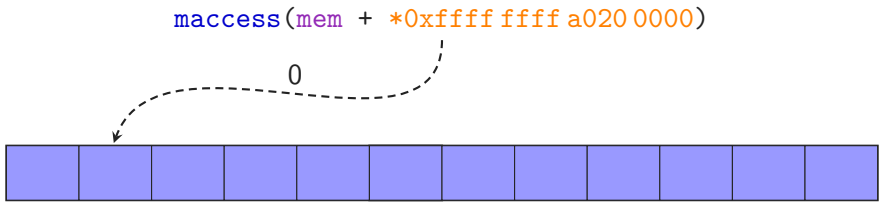
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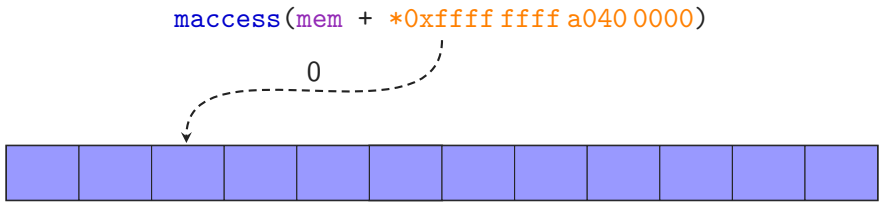
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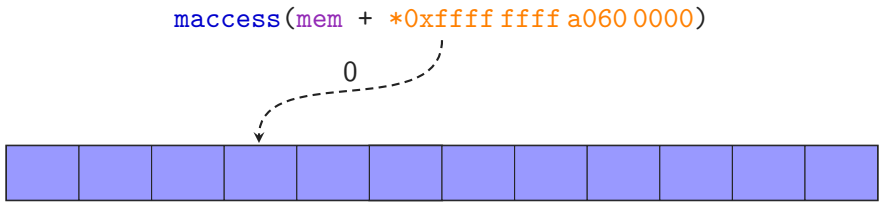
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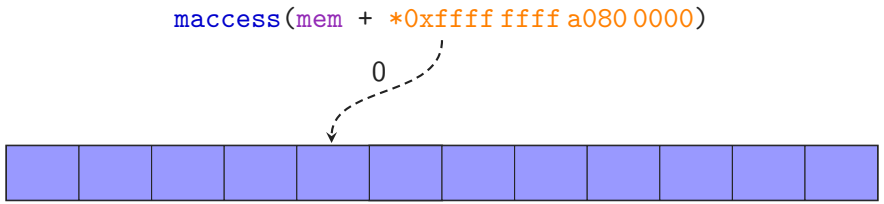
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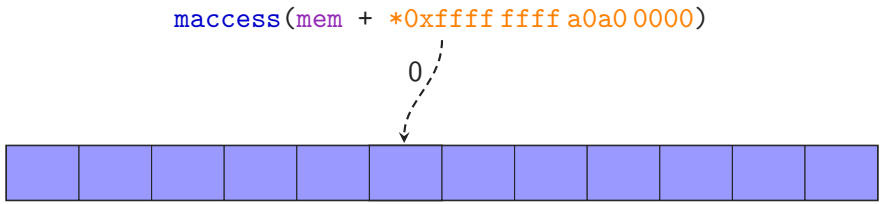
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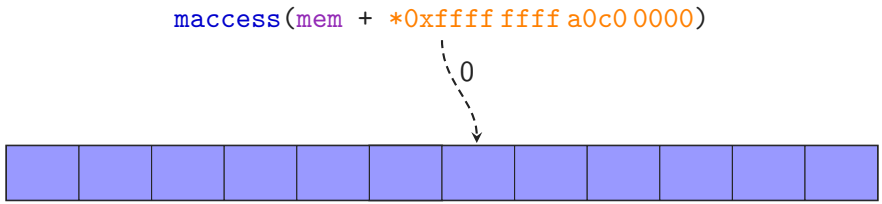
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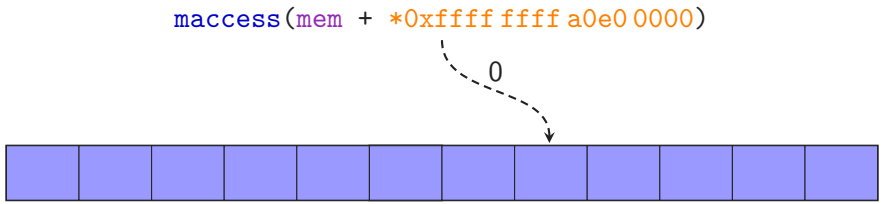
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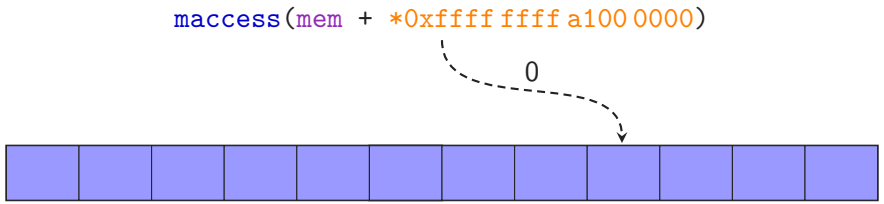
maccess(mem + *0xffff ffff a100 0000)
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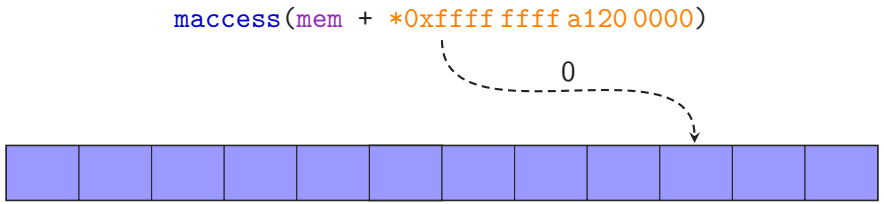
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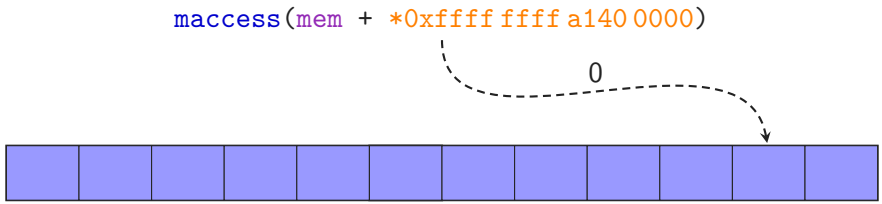
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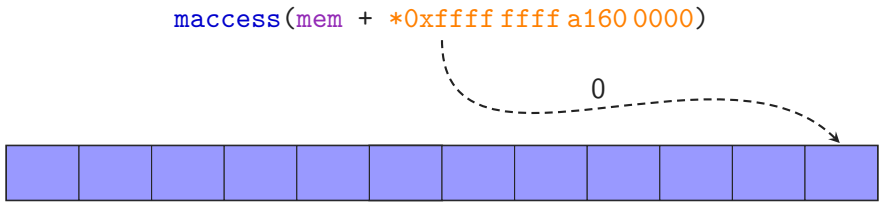
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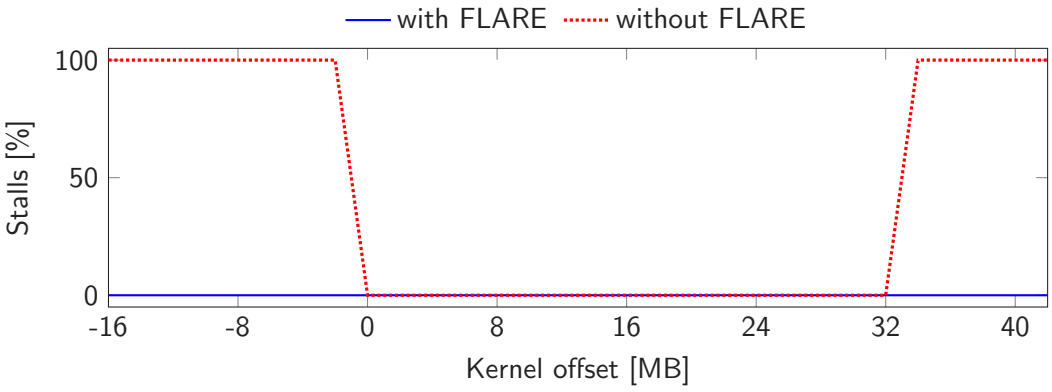
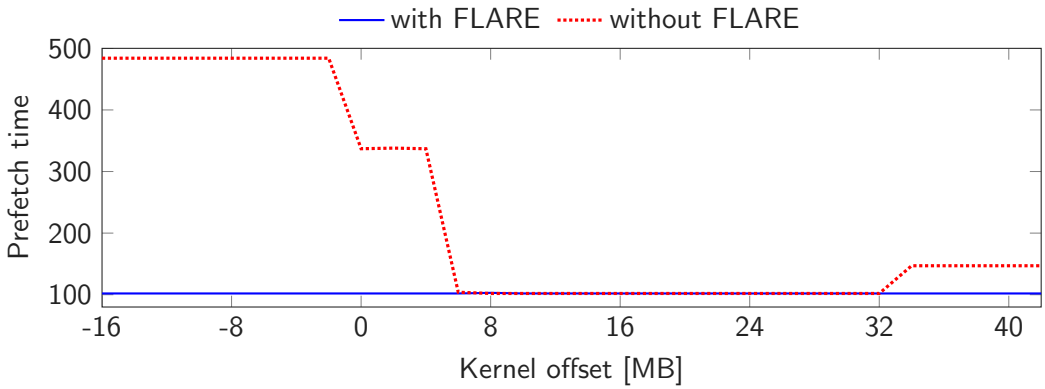
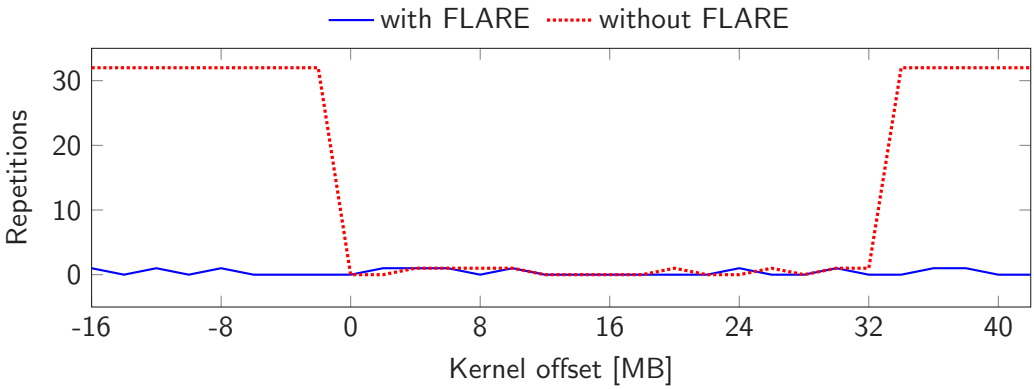

with FLARE
without FLARE
100
50
0
Stalls [%]
-16
-8
0
8
16
24
32
40
Kernel offset [MB]

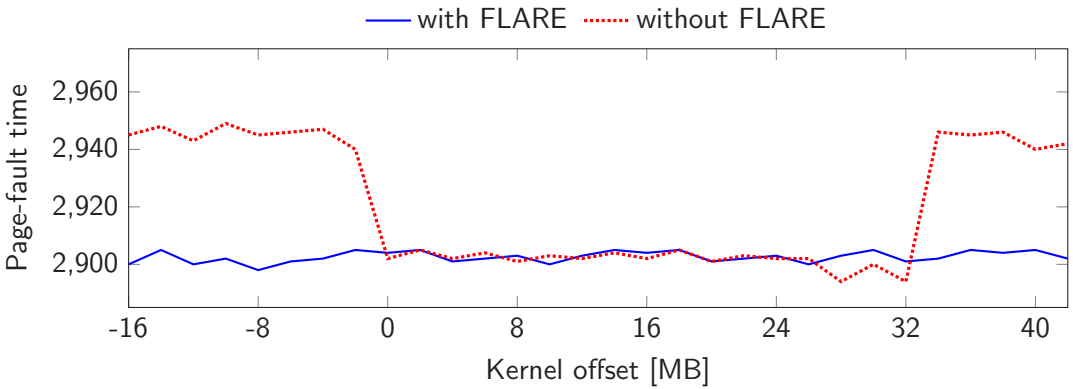
EchoLoad



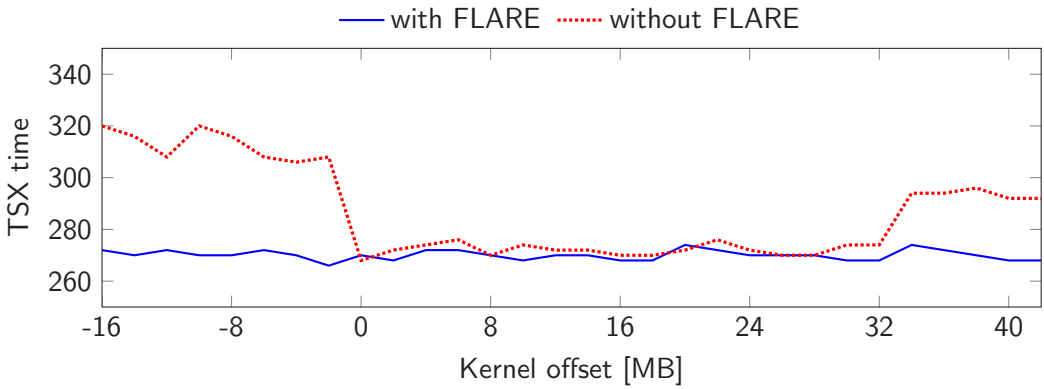
Prefetch [Gru+16]



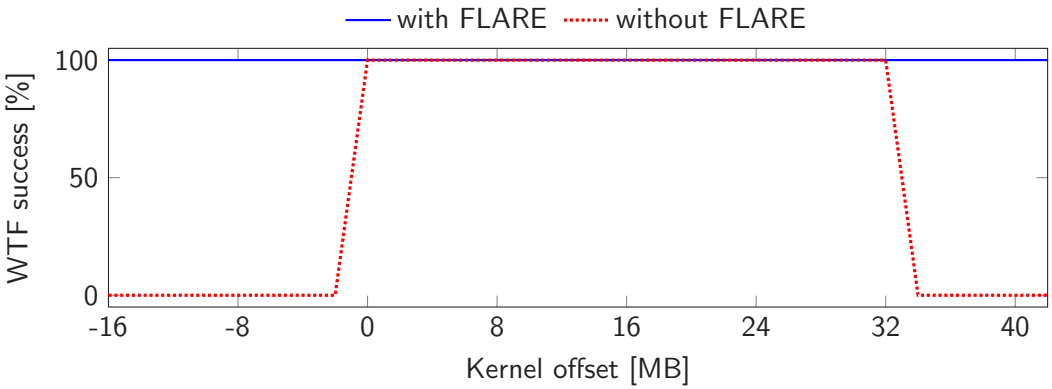
Data Bounce [Sch+19]



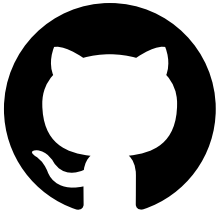
Double page fault [HWH13]


with FLARE
without FLARE
TSX time
340
320
300
280
260
-16
-8
0
8
16
24
32
40
Kernel offset [MB]

DrK [JLK16]



Fallout [Can+19]



You can find our proof-of-concept implementation of FLARE on:

- `https://github.com/IAIK/FLARE`

More Details

More details in the paper [Can+20]

- Attacks from and on SGX
- Meltdown in JavaScript
- Kernel modules, vmalloc, ...
- ...

AsiaCCS'20

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KASLR: Break It, Fix It, Repeat.

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→ Need to consider impact mitigations have on security

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References

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