Chip Impedance Characterization for Contactless Proximity Personal Cards

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***Abstract*—We present a new method to characterize impedance of proximity personal smartcard chips from low voltage up to destruction level. Our method is based on an extended setup using network analysis. Combined with antenna parameters, we relate the equivalent electrical chip parameters to transponder behaviour in the contactless system. The detailed considerations of this approach allow to verify and optimize chip design, operating software and inlay antenna production for an improved fit to application requirements.**

I. INTRODUCTION

Chip impedance measurement, more accurately the measurement of admittance, the equivalent parallel capacitance and parallel resistance at the antenna connection pins is important for chip manufacturers of contactless personal cards to verify their design. Moreover, chip impedance is the complementary part to loop antenna design, which allows inlay manufacturers and system integrators to meet application requirements for their contactless transponder product. However, concerns to several aspects may arise, even if we agree to this first, basic statement. Contactless card technology operating in the 13.56 MHz frequency band is well-known with billions of cards in the field up to date. Instruments for LCR measurement are available and in place today, and the measurement seems to be straightforward. So what is the reason to implement something new?

First of all, we found there is no instrument available or in place at the main companies allowing impedance measurements at 13.56 MHz frequency at output voltages exceeding 2 V(rms). However it is desirable to characterize the chip not only in a switched off state, but of even greater importance under operating conditions, even up to the destruction level, to verify essential operating points. In this context it should be known that the clock frequency for operation is usually derived from the AC input signal. To increase the measurement AC voltage with a DC offset or to measure at a lower frequency can lead to different operating conditions and to different parasitics, so this cannot be a general solution.

One may also mention, Radio Frequency Identification (RFID) in the UHF-band (840 – 960 MHz in this context, free bands depending on national frequency regulation) is in general more interesting and promising. Impedance characterization for UHF RFID is more challenging, supported by a larger number of actual publications.

In fact, it is true, that the main challenges to characterize UHF chip impedance, like to consider and compensate parasitics of the measurement setup and to measure small capacitance values of 1 – 3 pF, are relaxed for 13.56 MHz systems. On the other hand, there are different problem aspects, e.g. de-tuning caused by close coupling for resonance frequency measurement, or the higher operating voltage and power. Low power design is a key factor for all battery-less and contactless technologies, but there still are orders of magnitude between the power available for an UHF tag in several meters distance to the reader, in the range of some microwatts, and around 10 milliwatts for a contactless personal card powered by the H-field in 10 cm distance to the reader, which must even be able to thermally survive more than 250 mW under good coupling conditions. This power is invested to operate a microcontroller at clock frequencies in the range of 100 MHz, allowing advanced algorithms for secure transmission of personal data content in real time. In this regard the contactless feature is not only just another interface, but actually the basis of this battery-less technology, to which all other features must be compliant to and be characterized for.

In general, it is no question that the principle of inductive coupling is known and good models already exist [9]. However, new, promising approaches like smaller antenna sizes or Very High communication Data rates (VHD) in the range of 10 Mbit/s require to re-fine the models and also to take aspects of a second order into account. Accuracy and tolerance considerations are more in focus, to optimize systems over production tolerances. Considerations taken from conventional communication technology, relating an increase of data rates directly with higher bandwidth demand and higher carrier frequencies are not sufficient in this context. Seen from the energy point of view, for battery-less secure contactless proximity devices, the 13.56 MHz technology may be more promising, as it will be easier to improve data transmission, than to decrease the energy consumption for security in this extent. The huge number of installed terminals and already available infrastructure is both an opportunity and challenge for a smooth intruduction of such new features, as it requires devices which must fit into the existing systems.

II. THE MEASUREMENT CONCEPT

A. Measurement Setup

Our setup consists of an Analyzer which allows to connect an external directive coupler for network analysis. Since the RF generator output level of all measurement instruments is low, this approach has the advantage that the measurement can be performed at higher power levels, if an amplifier is inserted between the Analyzer RF output

and the input of an appropriate high power directive coupler. The instrument measurement input ports must be protected by appropriate attenuation. It is good practice, to use overdimensioned power and attenuators, to linearize the system and improve the 50 Ohm matching. Figure 1 shows a schematic of the setup, and table 1 lists the instruments used.

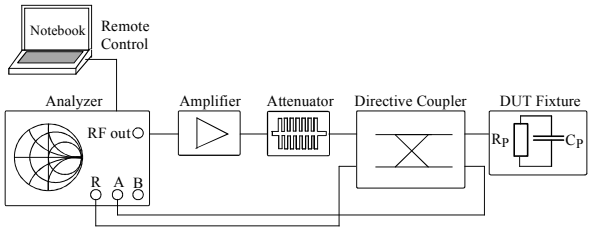

Figure 1. Setup for Chip Impedance measurement.

TABLE I. SETUP COMPONENTS

Component	Specification
Analyzer	Agilent 4395A
Amplifier	AR 75A250 (75 W, 250 MHz)
Attenuator	6 dB / 100 W
Directional Coupler	BDC 0100-40/200 (200 W, 40 dB)

Like in conventional network analysis, the analyzer measures the magnitude and phase of the reflection coefficient Γ_C as a ratio between the reflected and the foreward voltage signal, provided by the directional coupler. The absolute power level is not considered, and the instrument input ports must be protected by appropriate attenuation. Before measurement, the instrument is calibrated with open, short and 50 Ohm load references at the connection point to the test fixture at one (comparatively low) power level. Additional capacitance of the fixture socket is corrected separately.

The Smith Chart, introduced by Phillip Smith in 1939, gives a good impression about the measurement accuracy; it relates the reflection coefficient Γ to impedance Z by scaling. The analytical formula for chip impedance Z_C is

$$\underline{Z}_C = \frac{1+\underline{\Gamma}_C}{1-\underline{\Gamma}_C} Z_0 = \frac{1}{\underline{Y}_C}, \qquad (1)$$

where Z_0 is the 50 Ohm line impedance. The equivalent parallel resistance and capacitance are calculated by the instrument according to

$$R_P = \mathrm{Re}\{\underline{Z}_C\} = \mathrm{Re}\left\{\frac{1}{\underline{Y}_C}\right\} = \mathrm{Re}\left\{\frac{1}{G_P + jB_P}\right\} = \frac{1}{G_P} \qquad (2)$$

$$C_P = \mathrm{Im}\left\{\frac{1}{\underline{Y}_C}\right\} = -\mathrm{Im}\left\{\frac{1}{2\pi f_{MEAS}\,\underline{Z}_C}\right\} = \frac{B}{\omega}. \qquad (3)$$

B. Voltage on DUT

One critical point for this measurement is to relate the equivalent measured admittance values to a voltage applied on the Device Under Test (DUT). Direct measurement with a scope and probe in parallel to the chip can be problematic, because it requires an additional instrument. The voltage readout contains additional errors, and most important, this additional device may introduce additional measurement errors. Since the Analyzer can also be used to measure voltages (it has a Spectrum Analysis mode, like most Analyzers), it can be used to measure the output voltage of the directive coupler in a first step. Then the voltage on each DUT during admittance measurement can be calculated based on voltage dividers. Of course, this requires that the setup does not change properties (like amplifier gain) over time, so it is good practice, to let all instruments warm up for 20 minutes before starting the actual measurement.

The output of the directional coupler can be modeled as an internal AC voltage source and a serial 50 Ohm output resistance. In the prepared setup this output is connected to the 3rd Analyzer input port, which also has 50 Ohm impedance, so the source voltage will be twice as high as the measured voltage. We can relate the instrument RF output power (controlled by the instrument) to this measured source voltage U_S at the point for the DUT.

The admittance measurement can be performed as a power sweep at 13.56 MHz. The voltage amplitude at the DUT can be calculated for every point of the known U_S by

$$U_{DUT} = U_S \frac{R_C}{\sqrt{(R_C + R_S)^2 + (\omega R_C R_S C_C)^2}}. \qquad (4)$$

Here, R_C is the equivalent parallel chip resistance, R_S is the 50 Ohm source resistance, and C_C is the equivalent parallel chip capacitance.

III. CONSIDERATIONS ON CHIP NETWORK AND MEASURED TRACES

A. Chip Architecture

A simplified equivalent functional circuit for an integrated Proximity SmartCard CMOS chip is given in fig. 2.

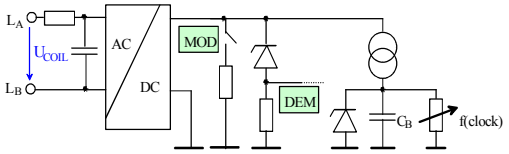

Figure 2. Simplified equivalent functional chip circuit.

The antenna coil connections L_A and L_B are the only two accessible pads of the chip, at which the admittance can be measured. An integrated resonance capacitance is connected over a serial resistance, which represents internal line resistance and filters. Different to front ends for UHF RFID, no charge pump is required to increase voltage, but a rectifier converts the 13.56 MHz AC voltage to DC.

Internally the voltage is limited by a shunt regulator and modern concepts include two (or more) stabilized voltage levels. The digital part operates on a low voltage level, and like for all CMOS oscillators, the current consumption is a function of the internal clock frequency, and it is smoothed by a buffer capacitor. Only if sufficient current is available, a reset condition will be removed, to assure proper function. Higher input power will be limited on a higher voltage level, which can also serve for analogue functions like the demodulator for reader commands. Load modulation is achieved by switching on and off a parallel shunt resistor. This change in current consumption modulates the transponder Q-factor and means intentional, modulated de-tuning of the reader antenna in the proximity coupling system.

B. *Measured resistance and capacitance traces*

Traces for equivalent parallel resistance and capacitance for an ISO/IEC14443 compliant SmartCard chip engineering sample measured with a method and setup described in chapter 2 are shown in figure 3 and 4. For comparison, the same chip sample was measured with an HP4194A LCR-meter.

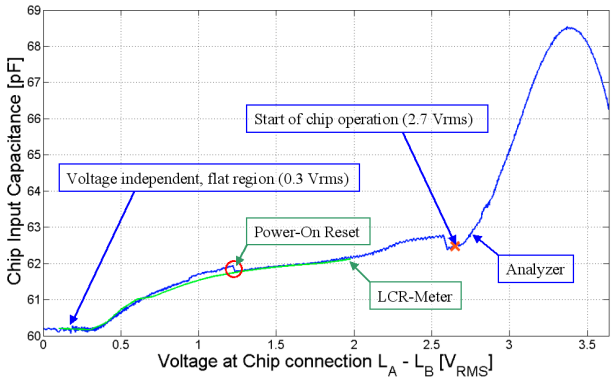

Figure 3. Measured equivalent parallel chip capacitance trace.

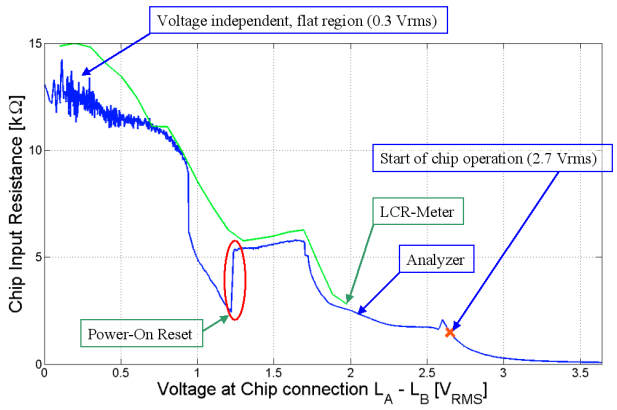

Figure 4. Measured equivalent parallel chip resistance trace.

To explain the trace, we can start at low voltage. Up to 0.4 V(rms) the input rectifier is in a non conducting state, so in this region (typically measured at 0.3 V(rms)) the capacitance and the resistance are constant. For increasing input voltage, the rectifier gradually becomes conductive and the voltage dependent parasitic capacitance increases. In fact, the exact voltage levels and resistance values in this region show statistic variations, because they depend on the charge in parasitic capacitances on Mosfet gates. The first circuit to react in all cases is the power on reset. This part is designed to operate at the lowest possible voltage, and to set all other blocks to a defined reset, which means a steep increase in the resistance. The voltage can then be further increased up to the point for a first stabilized voltage. Circuits for chip security will be activated in this region, and with increasing voltage, the available current increases up to a defined point, at which the controller processing unit (CPU) will be switched on. As the CPU current consumption is a function of the clock frequency, this point will depend on the chip operation settings. Our measurements presented here were performed on one engineering sample, a chip in development phase, so the values (capacitance, resistance, voltage levels) will be similar, but not equal to an existing product. For our engineering sample, we measure about 1500 Ohms at 2.7 V(rms) for this point. As can be seen, this also means a dip in the trace for the equivalent parallel capacitance of the chip. Further inrease of the voltage will cause the main voltage limiter to increase the current by adjustment of a shunt, which keeps the internal voltage almost constant for the digital part, but the voltage drop on the rectifier increases, which allows some increase in the measurement voltage applied on the chip. While the equivalent parallel resistance drops, the equivalent capacitance increases significantly.

The comparison shows a good fit of the capacitance traces measured with both instruments in the overlapping voltage range up to 2 V(rms). This gives confidence that the new method will also deliver accurate values for the most interesting part of the curve, the chip in operation, exceeding the LCR meter voltage range. 19 points were measured with LCR meter, and 1200 points were measured with the Analyzer method, which may explain, why the power on reset is not seen in the LCR meter trace.

IV. Relating Chip Impedance with Contactless Measurements

We can use a model for contactless transponder properties and apply the contact-based chip impedance measurement. This actually is the aim of the measurement, as it allows further considerations on allowable parameter changes for chip and antenna (e.g. considerations on allowable tolerances, or an optimization of the operating software for a specific contactless application). Test methods and a specific antenna arrangement for contactless characterization of Proximity transponders compliant to the ISO/IEC14443 base standard are defined in ISO/IEC10373-6, and we will use the same test equipment as it is typically available and also required for product certification. Some properties of this test bench are explained in [8]. We will calculate a trace for the minimum H-field required for chip operation, marked with an "x" in fig. 3 and 4.

TABLE II. List of Parameters for Antenna and Chip.

Parameter	Meaning	Unit	Value
f_{CAR}	carrier frequency	MHz	13.56
R_{C0}	eq. parallel chip resistance (measured at 0.3 Vrms)	Ohm	14000
R_{C1}	eq. parallel chip resistance at start of operation (at 2.7 Vrms)	Ohm	1500
U_{MIN}	voltage for start of chip operation	V(rms)	2.7
L_F	inductance of fixture (Cal. Coil)	Henry	2×10^{-7}
L_S	inductance of one Sense Coil	Henry	4.2×10^{-7}
L_A	inductance of card antenna	Henry	1.86×10^{-6}
k_{AF}	coupling factor antenna - fixture	---	0.115
k_{AS}	coupling factor Sense Coil - antenna	---	0.22
R_{SA}	eq. serial antenna resistance (measured at 13.56 MHz)	Ohm	1.7
A	antenna area	m²	0.0014
N	loop antenna turns	---	3.8

In a good chip design, the minimum H-field will be determined by the energy requirement of the chip, not by a communication fail for low H-field strength. Still we have to consider 3 phases in communication, each of these may be the limiting aspect:

- Phase 1 is the communication of reader to card, which means the 13.56 MHz carrier is modulated by pulses to transmit the reader command.
- Phase 2 means data processing on the transponder chip, while the carrier is not modulated.
- Phase 3 is transponder load modulation. An additional shunt is nearly shorting the antenna at a certain duty cycle, which also means reduced energy reception for the chip.

In our case, phase 2 will be the limiting factor, so the minimum H-field as function of the transponder resonance frequency can be well described by the formula

$$H_{MIN} \cong \frac{\sqrt{\left[1-\left(\frac{f_{CAR}}{f_{D1}}\right)^2\right]^2+\left(\frac{2\pi f_{CAR} L_A''}{R_P}\right)^2}}{2\pi f_{CAR}\,\mu_0\,N\,A}\cdot U_{MIN} \qquad (5)$$

Transponder resonance frequency is one important elementary parameter. According to compliance test definitions, the transponder resonance frequency is measured separately in a contactless mode, with an analyzer and a loop coil as fixture. The fixture is compensated (without DUT) and the resistance trace maximum allows to read out the resonance frequency. Obviously, it will change with the chip capacitance as a function of coil voltage, so it is one very tricky aspect in practice, to measure the resonance frequency at the right operating point, as the analyzer has no option to apply or detect modulation. For our consideration, we measured the transponder resonance frequency at low H-field conditions (generated by setting a low output voltage of the analyzer, connected to the fixture coil) and at a defined distance to the fixture coil. This corresponds to a low coil voltage < 0.3 V(rms) which has the advantage, that the chip capacitance and resistance are independent of (small scale) voltage changes, and the Q-factor is highest which allows easy read-out. Simple but useful for overview considerations is the Thomson equation for the resonance frequency of a parallel LCR-resonator. It is given by

$$f_1 = \frac{1}{2\pi\sqrt{LC}}\cdot \qquad (6)$$

However, as we aim to be more accurate, we have to take into account at least two more aspects, to relate chip impedance to transponder resonance frequency.

A. *Serial resistance in antenna and assembly*

In practical cases, we may observe significant additional serial resistance between chip and antenna, which can either be caused by the chip assembly (e.g. for conductive glueing to the antenna) or by a low antenna Q-factor (e.g. for printed coil technology).

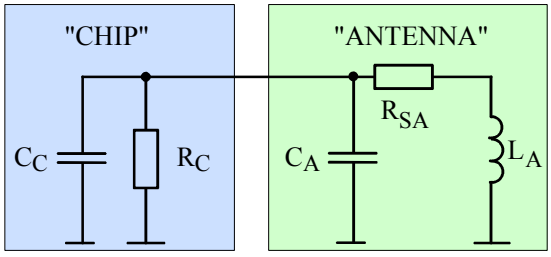

Figure 5. Equivalent circuit for chip and antenna.

An equivalent circuit for this case is given in fig. 5, and the resonance frequency is shifted to a higher value according to

$$f_{RES} = \frac{1}{2\pi}\sqrt{\frac{R_C + R_{SA}}{L_A(C_C + C_A)R_C}} \qquad (7)$$

B. *Frequency shift caused by close coupling between coils*

Close coupling is an aspect related to the proximity of loop coils, which results in a change of inductance for both coils, and resonances for both. A detailed explanation is given in [6]. For the transponder this causes a resonance frequency shift. In our measurement, we have to take into account two such scenarios:

- In resonance frequency measurement, coupling to the fixture coil results in a resonance frequency measured *lower* than the natural frequency, and
- In minimum H-field measurement the coupling to the sense coil in the ISO/IEC10373-6 setup also shifts the transponder resonance down. This means the minimum required H-field is achieved accordingly for a natural transponder resonance frequency *higher* than the carrier frequency of 13.56 MHz.

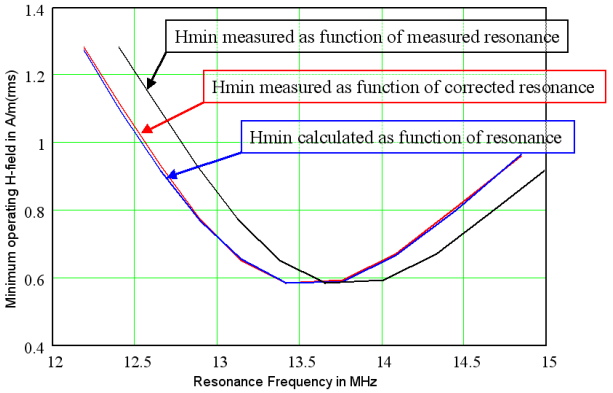

Figure 6. Minimum required H-field over transponder resonance.

We can calculate the natural transponder resonance frequency f_T from the detuned, measured resonance frequency f_M at low H-field conditions (index 0).

$$f_{T0} = \sqrt{L_A' \cdot \frac{R_{C0} + R_{SA}}{R_{C0}\,L_A}}\cdot f_{M0} \qquad (8)$$

where the new, reduced antenna inductance is given by

$$L_A' = \frac{L_A + L_F}{2} + \sqrt{\frac{(L_A + L_F)^2}{4} - \left(L_A L_F - k_{AF}^2 L_A L_F\right)} \qquad (9)$$

Then we can calculate the natural transponder resonance frequency in the intended operating point (index 1) from our measurement of equivalent parallel chip capacitance, according to

$$f_{T1} = \frac{1}{2\pi}\sqrt{\frac{R_{C1} + R_{SA}}{R_{C1}L_A\left[\frac{R_{C0} + R_{SA}}{R_{C0}L_A(2\pi f_{T0})^2} + \Delta C_C\right]}} \qquad (10)$$

Finally, the detuned resonance frequency of the transponder in the ISO/IEC10373-6 antenna arrangement,

for H-field conditions in the intended operating point can then be calculated according to

$$f_{D1} = \frac{1}{2\pi\sqrt{L_A'' \cdot \frac{R_{C1} + R_{SA}}{R_{C1} L_A (2\pi f_{T1})^2}}} \quad (11)$$

where the modified antenna inductance due to coupling to the sense coil is given by

$$L_A'' = \frac{L_A + 2L_S}{2} + \sqrt{\frac{(L_A + 2L_S)^2}{4} - \left(L_A 2L_S - k_{AS}{}^2 L_A 2L_S\right)} \quad (12)$$

With these corrections to the resonance frequency, the measured minimum H-field required for the transponder to start operation can be related to the calculated curve based on chip impedance and antenna parameters.

The transponder Q-factor can be calculated according to

$$Q_T = \frac{R_P}{2\pi f_{RES} L_A} = \frac{2\pi f_{RES} L_A R_{C1}}{(2\pi f_{RES} L_A)^2 + R_{C1} R_{SA}} \quad (13)$$

where L_A changes to L_A'' in the ISO/IEC10373-6 setup.

C. Application Aspects

Once the model fits so accurately to the measurement, it can be used to answer several interesting application related aspects.

One important aspect are production tolerances for the final product. Given a maximum allowable value for Hmin (e.g. determined by certification requirements), the minimum and maximum allowable resonance frequency in the ISO/IEC10373-6 setup (14 and 15) and for resonance frequency measurement on the analyzer can be determined.

$$f_{MIN} = \frac{f_{CAR}}{\sqrt{1 + \sqrt{\left(\frac{H_{MIN} 2\pi f_{CAR} \mu_0 NA}{U_{MIN}}\right)^2 - \left(\frac{2\pi f_{CAR} L_A''}{R_P}\right)^2}}} \quad (14)$$

$$f_{MAX} = \frac{f_{CAR}}{\sqrt{1 - \sqrt{\left(\frac{H_{MIN} 2\pi f_{CAR} \mu_0 NA}{U_{MIN}}\right)^2 - \left(\frac{2\pi f_{CAR} L_A''}{R_P}\right)^2}}} \quad (15)$$

This allows to specify production tolerances for chip and antenna parameters for the application. Alternatively, based on a given variance of every parameter, a Monte Carlo simulation can give a typical distribution for the minimum required H-field for the final product.

Another aspect concerns the operating software of the chip. The question, how much current is required is heavily dependent on the implementation of the software; in which order some steps are performed, and to which clock frequency the chip is set. This allows to optimize execution time and security level for the application requirements, as it relates the analogue properties of the personal card in a predictable way to the program. Similar considerations in chip architecture are a vital part for the implementation of VHD up to 10 Mbit/s.

In the same way, it is possible to optimize antenna design (e.g. smaller antennas) to chip properties. If a higher transponder Q-factor is applied, in principle a smaller antenna can deliver equal current than a larger antenna to supply the chip (for a reader with larger antenna, the so-called "card loading effect" will also be similar then), but transponder production tolerances must be reduced, which will require more accurate measurements for production quality control and may even need a costly tuning step in the production process.

V. Conclusions

We have used an extended setup for network analysis in a new application, to characterize the equivalent input impedance of a contactless smartcard chip over the complete operational range. We have introduced a refined model to calculate the minimum H-field strength over resonance frequency required for transponder operation and we have validated this measured impedance by both, minimum H-field measurement and analytical calculation.

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