Medha: **M**icrocoded **H**ardware **A**ccelerator for computing on **E**ncrypted **D**ata

Cryptographic Hardware and Embedded Systems (CHES), 2023

Ahmet Can Mert[1], **Aikata**[1], **Sunmin Kwon**[2], **Youngsam Shin**[2], **Donghoon Yoo**[2], **Yongwoo Lee**, **Sujoy Sinha Roy**[1]

[1] IAIK, Graz University of Technology, Graz, Austria
[2] Samsung Advanced Institute of Technology, Suwon, Republic of Korea

Outline

1. Motivation and Background
2. Microcoded Hardware Accelerator
   - Architecture of homomorphic processor
   - FPGA implementation with placement-friendly layout
3. Evaluation Results

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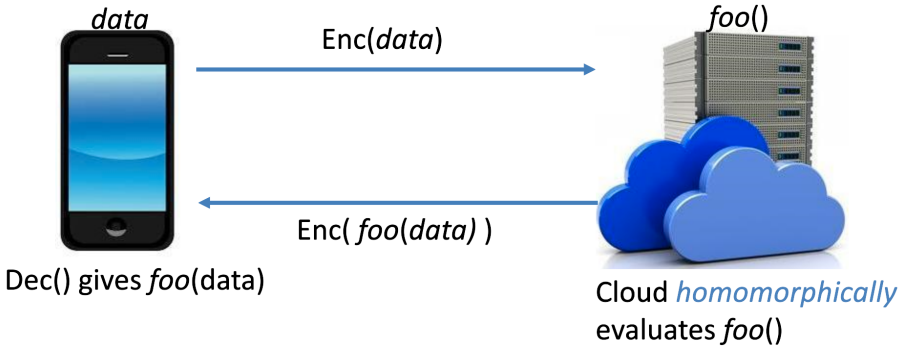
Homomorphic Encryption

Homomorphic Encryption (HE) allows computation on the encrypted data.



Challenges in accelerating Homomorphic Encryption

1. Computationally intensive:

10^4 to $10^5\times$ plain computation

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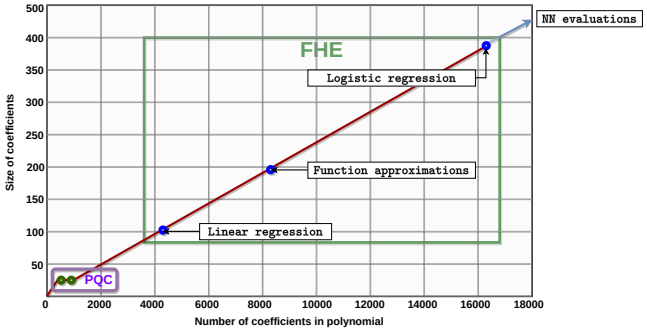

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   - Long integer arithmetic
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$$\mathbb{O}(N^2) \rightarrow \mathbb{O}(N \log_2 N)$$

Challenges in accelerating Homomorphic Encryption

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   - Long integer arithmetic $\leftarrow$ RNS
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$$\boxed{Q \rightarrow \prod_{i=0}^{L-1} q_i}$$

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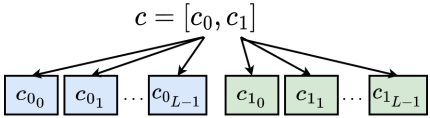

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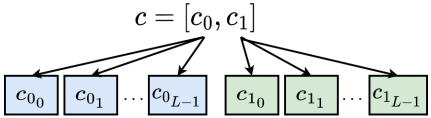

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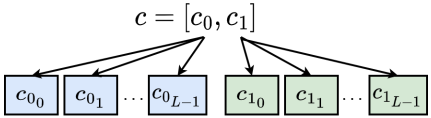

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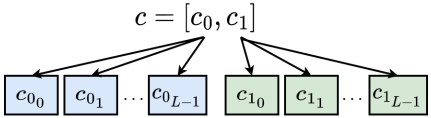

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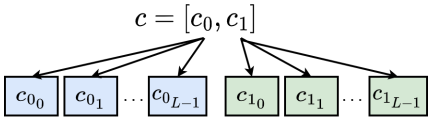

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    (Base conversion: NTT $\rightarrow q_i$ to $q_j \rightarrow$ INTT)

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Our Solution: **Medha**

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An Overview of HW-based HE accelerators in the literature

Two main tracks:

1. Accelerator prototypes in FPGA/ASIC
2. Simulation model of accelerator

Accelerator prototypes in FPGA/ASIC
HEAWS[TRV20], HEAX[RLPD20], CoFHEE[NSA+23]

Simulation model of accelerator
F1[FSK+21], BTS[KKK+22], CraterLake[SFK+22]

[TRV20] Furkan Turan et al. HEAWS: an accelerator for homomorphic encryption on the amazon AWS FPGA. IEEE ToC, 2020.
[RLPD20] M. Sadegh Riazi et al. HEAX: an architecture for computing on encrypted data. ASPLOS 2020.
[NSA+23] Mohammed Nabeel et al. CoFHEE: A Co-processor for Fully Homomorphic Encryption Execution. DATE 2023.
[FSK+21] Axel Feldmann et al. F1: A fast and programmable accelerator for fully homomorphic encryption. MICRO 2021.
[KKK+22] Sangpyo Kim et al. BTS: An Accelerator for Bootstrappable Fully Homomorphic Encryption. ISCA 2022.
[SFK+22] Samardzic et al. CraterLake: A Hardware Accelerator for Efficient Unbounded Computation on Encrypted Data. ISCA 2022.

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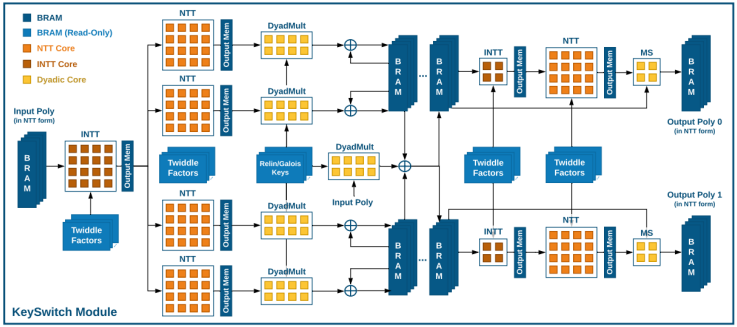
  - Sub-routine specific for HE



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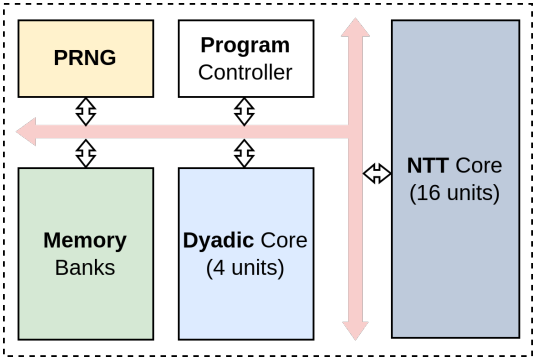

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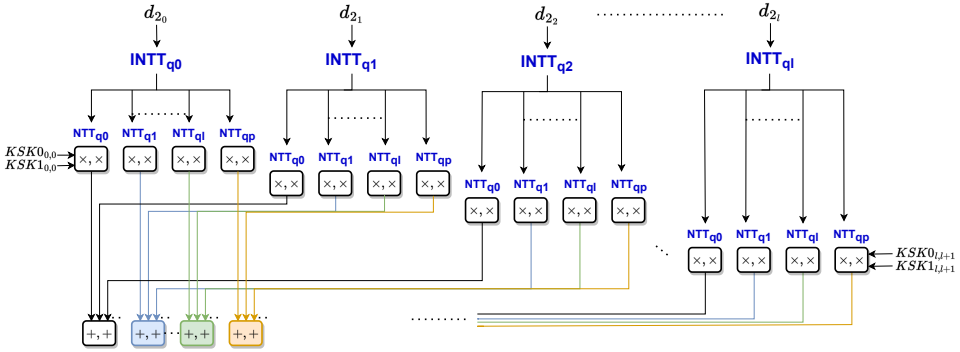

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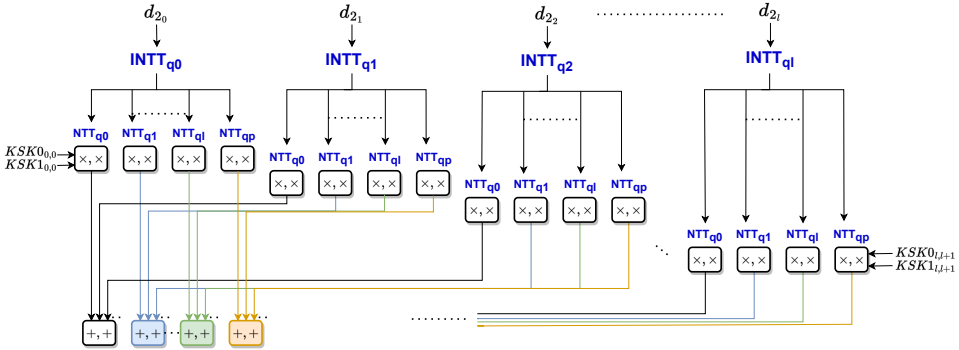

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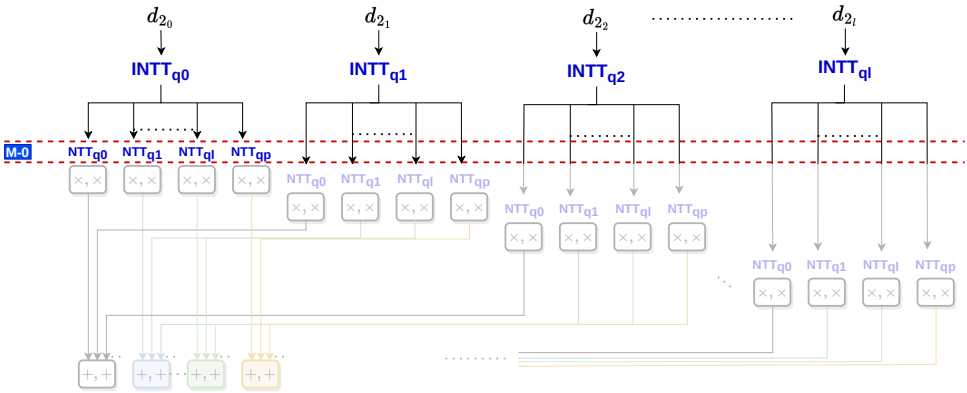

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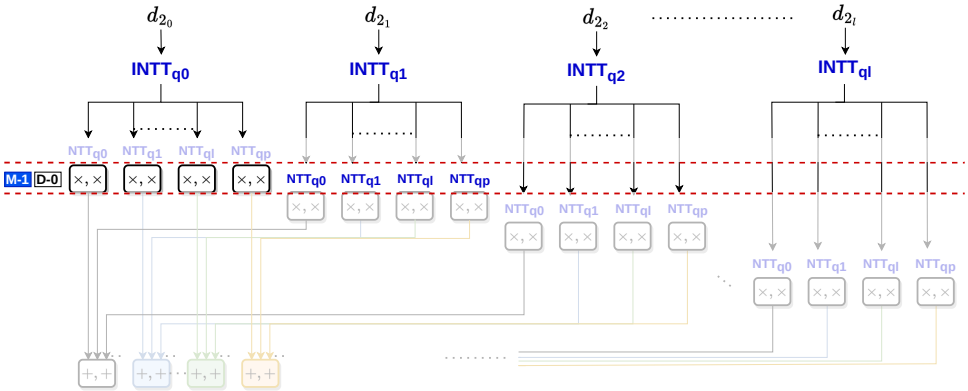

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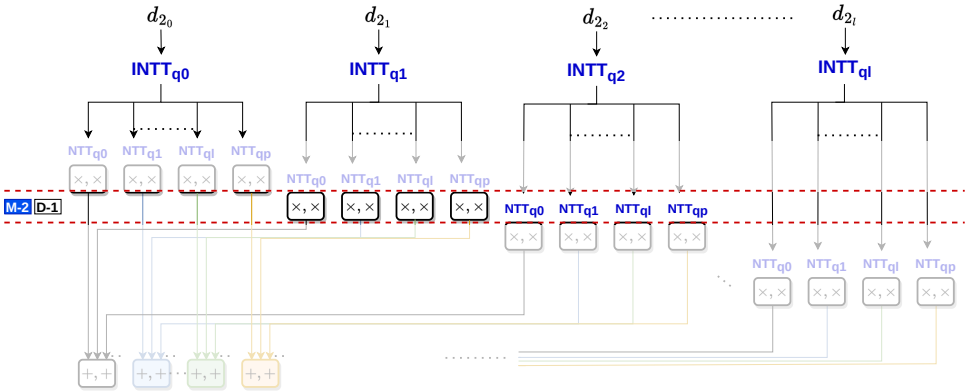

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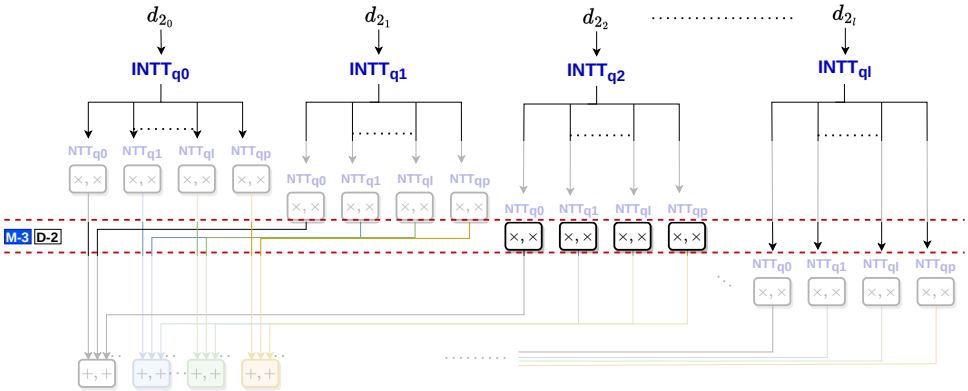

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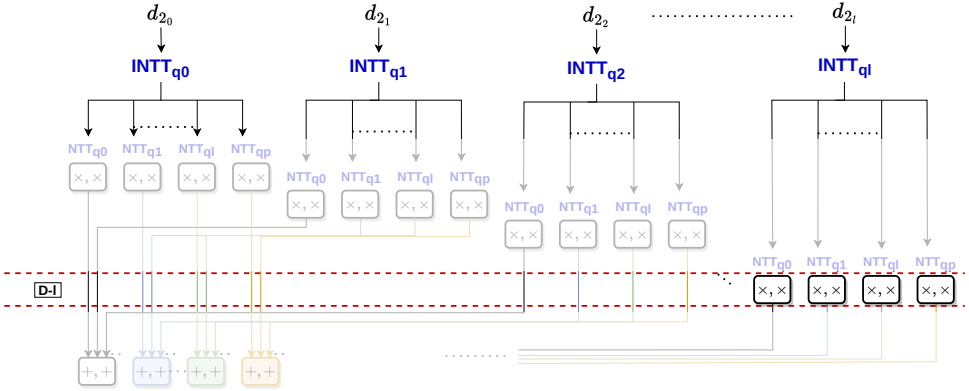

Parallel execution of NTT & dyadic cores results in significant cycle reduction!

Customized on-chip memory design

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Utilizing left-over bits in BRAM/URAM

- One URAM address can store 72-bits
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- One BRAM address can store 18/36/72-bits
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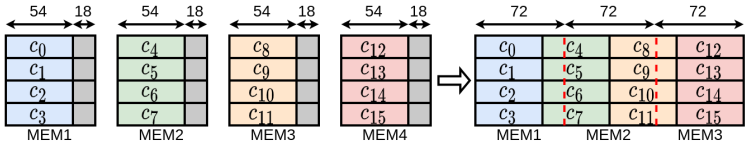
We created a virtual memory to utilize left-over bits in BRAM/URAM.

- Example: 54-bit coefficient storage in URAM



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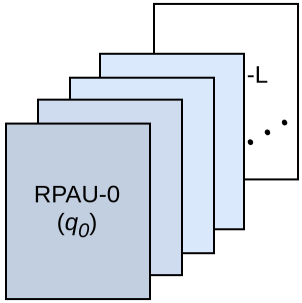

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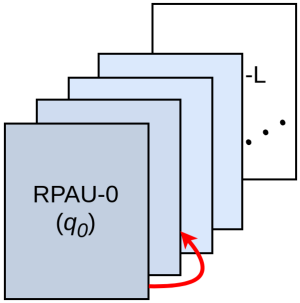

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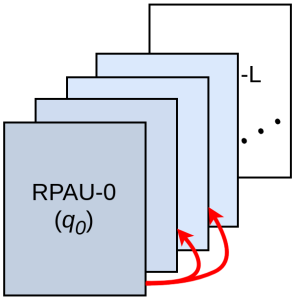

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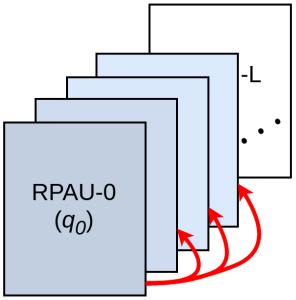

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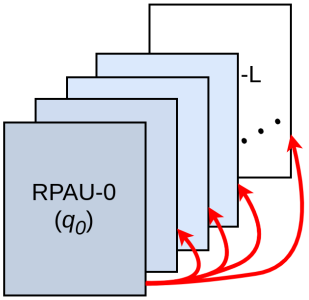

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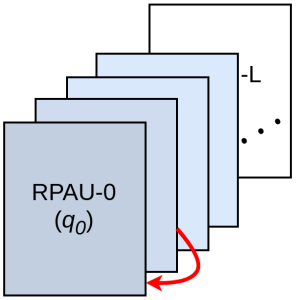

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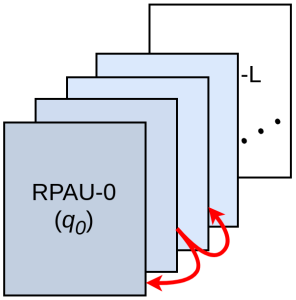

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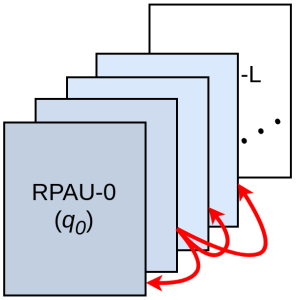

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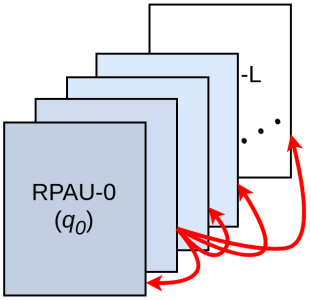

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2. Target platform (Xilinx Alveo U250 FPGA) constraints

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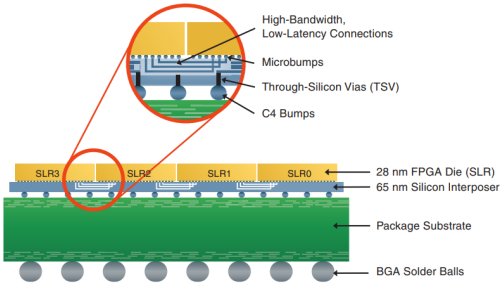

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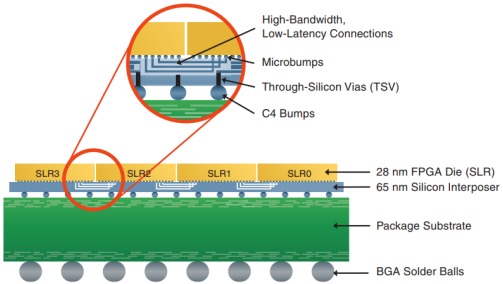

- Two neighboring SLRs are connected using a limited number of wires.

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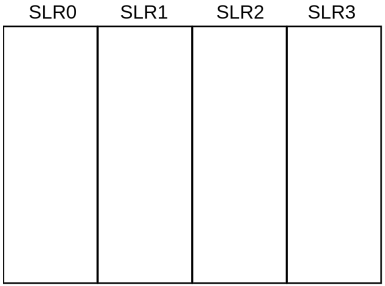

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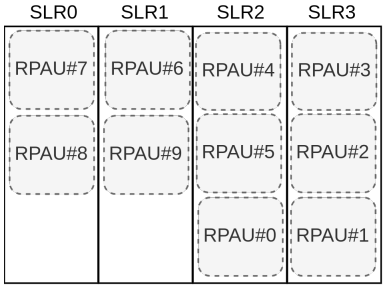

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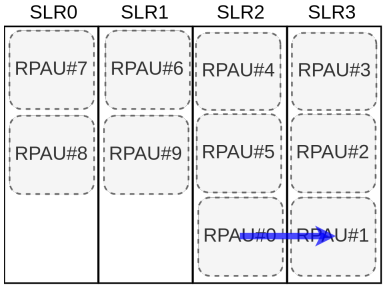

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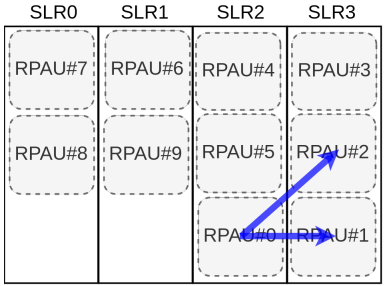

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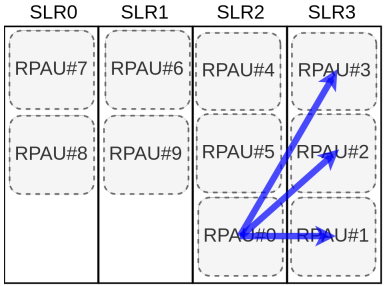

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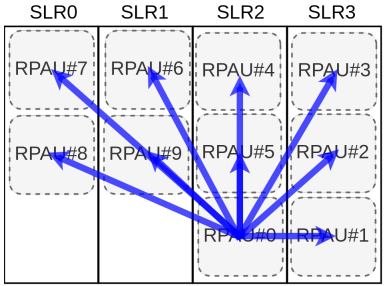

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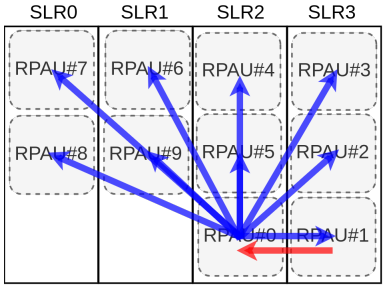

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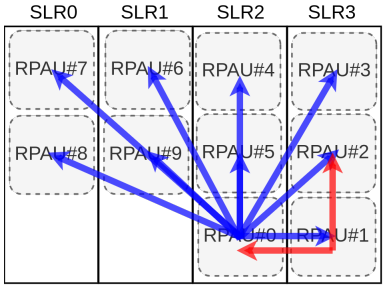

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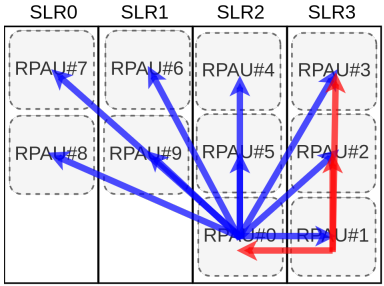

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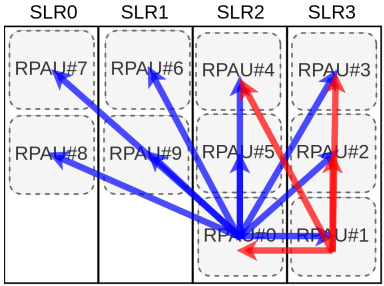

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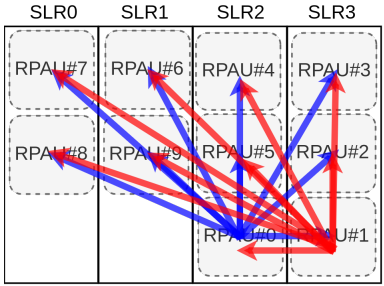

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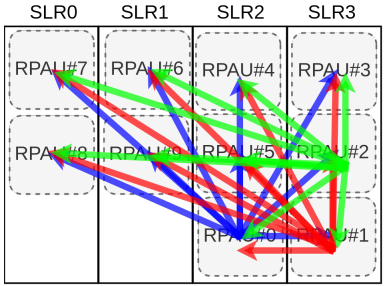

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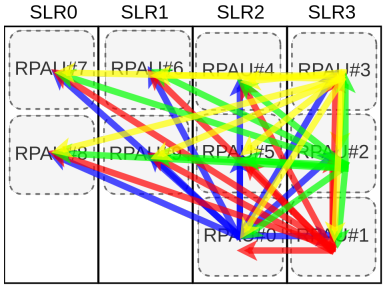

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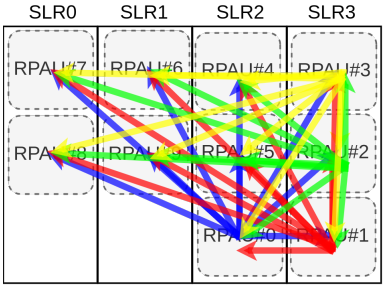

We need an efficient method to interconnect and map RPAUs!

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We must consider SLR-to-SLR connection constraints.

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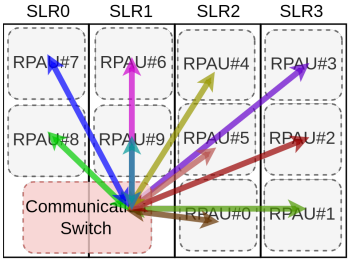

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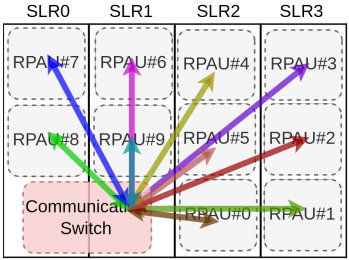

- Wiring complexity: $\mathbb{O}(L^2) \rightarrow \mathbb{O}(L)$
- Still many SLR-crossing nets

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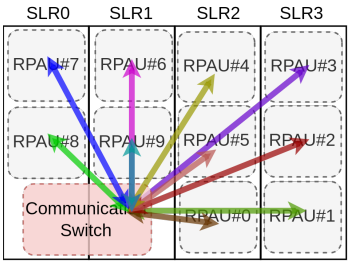

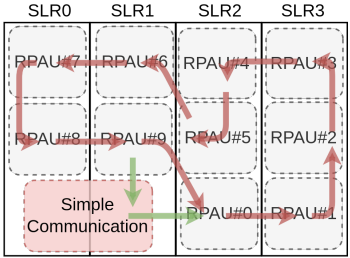

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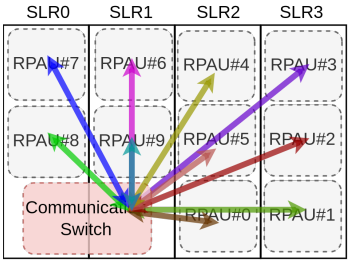

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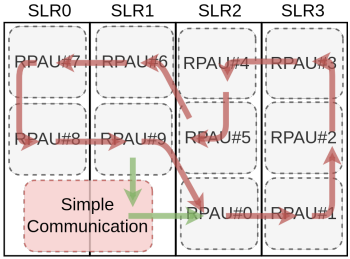


- Only neighbouring RPAUs connected
- Few SLR-crossing nets

Outline

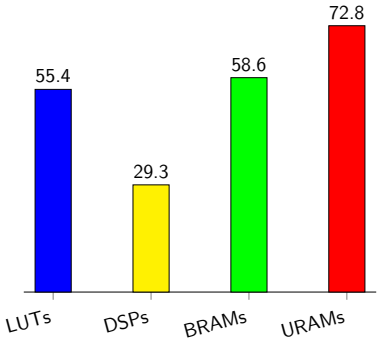
1. Motivation and Background
2. Microcoded Hardware Accelerator
   - Architecture of homomorphic processor
   - FPGA implementation with placement-friendly layout
3. **Evaluation Results**

Evaluation Results

As a proof of concept, our implementation employs 10 PEs and two parameter sets.

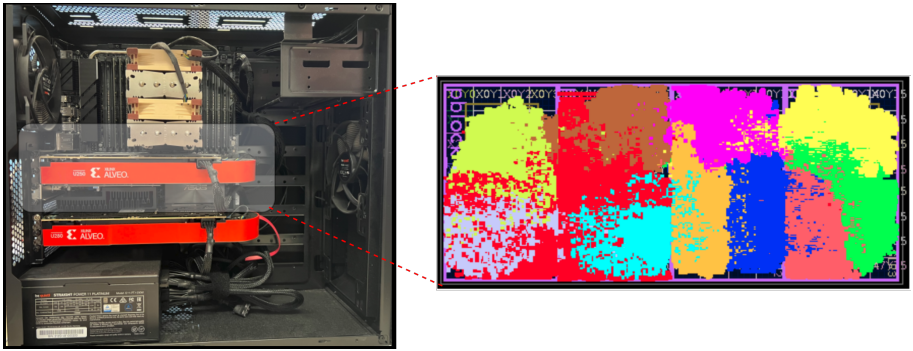
- **Set-1:** $\log_2(pQ) = 438,\ N = 2^{14}$
- **Set-2:** $\log_2(pQ) = 546,\ N = 2^{15}$

Resource utilization on Xilinx Alveo U250 FPGA (in %)



Evaluation Results

Placement of Medha on the Alveo U250 FPGA chip.



Evaluation Results

Performance on Alveo U250 board running at 200 MHz.

[SEA20] Microsoft SEAL (release 3.6). https://github.com/Microsoft/SEAL, November 2020. Microsoft Research, Redmond, WA.
[RLPD20] M. Sadegh Riazi et al. HEAX: an architecture for computing on encrypted data. ASPLOS 2020.

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  - Hom. Mult. + Relin. for Set-1: **497μ sec**
  - Hom. Mult. + Relin. for Set-2: **1,374μ sec**

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- Comparison with HEAX [RLPD20]
  - **2.3**$\times$ better latency

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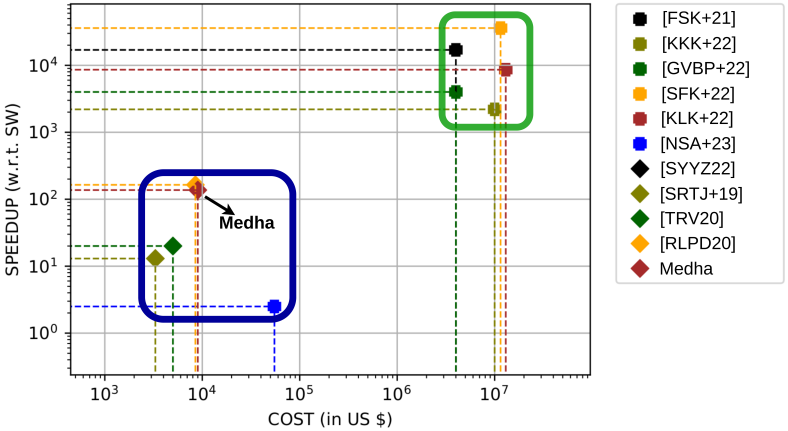

Medha: **M**icrocoded **H**ardware **A**ccelerator for computing on **E**ncrypted **D**ata

Cryptographic Hardware and Embedded Systems (CHES), 2023

Ahmet Can Mert[1], **Aikata**[1], **Sunmin Kwon**[2], **Youngsam Shin**[2], **Donghoon Yoo**[2], **Yongwoo Lee**, **Sujoy Sinha Roy**[1]

[1] IAIK, Graz University of Technology, Graz, Austria
[2] Samsung Advanced Institute of Technology, Suwon, Republic of Korea