Passive Component Optimization for Current-Source-Inverters

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***Abstract*—In addition to the actual semiconductor components and the cooling solutions required to dissipate losses, passive components account for a large part of the volume of power electronic converters. This publication presents methods for optimizing the volume or occupied PCB board area of the passive components of current source inverters (CSIs). For this converter topology, these are primarily composed of the filter capacitors placed on the output terminals and the DC-link inductance acting as the main energy storage device in the DC-link. Design equations for the design of these components are presented first. In addition to the basic relationships for determining the capacitance or inductance of the respective components, other constraints for their design are also taken into account. Furthermore, an optimization process is given for both the filter capacitors and the DC-link inductance, with which the volume or the occupied board area of the respective components can be designed as small as possible. On the basis of the optimization results for various input parameters, analytical relationships are then determined that can be used to quickly and easily estimate the volume and area at the beginning of a converter design process.**

***Index Terms*—Capacitors, converters, inductors, optimization, pulse width modulation converters.**

I. Introduction

THE development of SiC and GaN-based WBG semiconductor switches enables power electronic converters for variable speed drives (VSDs) and applications in power grids to operate at much higher switching frequencies than previously possible with conventional silicon (Si) based IGBTs and MOSFETs. Additionally, these new devices offer lower on-state resistance and thus lower conduction losses for the same chip size and, in the case of SiC, are better suited for operation at high temperatures (>150 °C) [2]. However, increasing the switching frequency of the commonly used voltage-source-converters (VSCs) and therefore the $\frac{dv}{dt}$ of the pulse width modulated output voltages not only offers advantages, such as a potential reduction of the size of passive energy storage components or filters used, but also leads to new challenges and risks [3], [4], [5]. These challenges caused by steep converter output voltage slopes can include, but are not limited to:

- Terminal overvoltages at the VSD if the converter and drive are connected by a long cable and there is a characteristic impedance mismatch between the two systems [4], [5], [6]. These can significantly stress or even damage the drive's insulation system.
- Emission of high-frequency electromagnetic disturbances violating electromagnetic compatibility standards [3].
- Increase in harmonic motor losses due to high-frequency output voltage components [7].

One way to address these problems is to use the increasingly popular current-source converter (CSC, see Fig. 1) topology [4], [8], [9], [10] instead of a VSC. In this case, an inductor is used as the main energy storage device in the DC-link which aims to maintain a constant average DC-link current while capacitors at the output provide an alternative current path for switching inductive loads. These components together possess the characteristic of a second-order filter which allows the generation of continuous rather than switched output voltages. In addition, this topology offers the potential of operation at high temperatures, since the CSC's passive components are usually much more temperature resistant than those of the VSC [4].

However, one major disadvantage of the CSC is that reverse-blocking (RB) or bidirectional (BD) switches have to be used for the main switching elements. To realize RB switches with

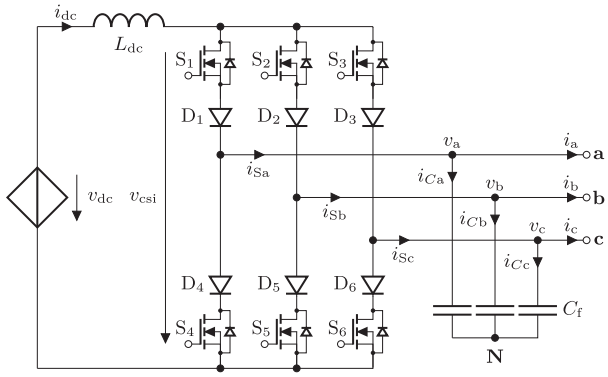

Fig. 1. Basic circuit diagram of the inverter side of a current source converter (current-source-inverter, CSI). The rectifier side is replaced with a controllable voltage source that aims to keep the DC-link current constant on average. Here, the reverse-blocking semiconductor switches are constructed from MOSFETs and diodes.

Manuscript received 30 November 2022; revised 31 March 2023; accepted 28 May 2023. Date of publication 5 June 2023; date of current version 20 September 2023. This work was supported in part by TU Graz Open Access Publishing Fund. Paper 2022-IPCC-1194.R1, presented at the 2021 IEEE Energy Conversion Congress and Exposition, Vancouver, BC Canada, Oct. 10–14, and approved for publication in the IEEE Transactions on Industry Applications by the Industrial Power Converter Committee of the IEEE Industry Applications Society [DOI: 10.1109/ECCE47101.2021.9595392]. *(Corresponding author: Benedikt Riegler.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIA.2023.3282565.

Digital Object Identifier 10.1109/TIA.2023.3282565

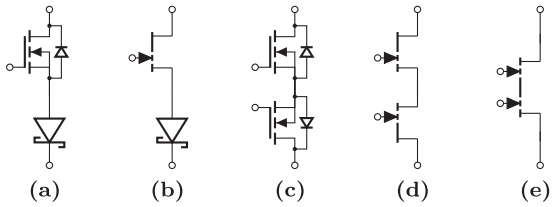

Fig. 2. Symbols of wide-bandgap material based reverse-blocking switch variants: (a) SiC MOSFET with SiC Schottky barrier diode, (b) GaN HEMT with SiC Schottky barrier diode, (c) Dual SiC MOSFET, (d) Dual GaN-HEMT, (e) BD GaN-HEMT.

available components, a conventional reverse conducting switch can be combined with a diode in series, which increases the circuit losses due to the forward voltage and reverse-recovery effect, or another antiserial switch. Fig. 2 depicts the circuit symbols of the different RB switch variants based on WBG technology such as SiC MOSFETs, GaN HEMTs, or SiC Schottky barrier diodes (SBDs). The symbol presented in Fig. 2(e) represents a dual-gate monolithic BD GaN HEMT that is promising for use in CSCs [9], [11], [12], [13], [14], [15]. However, these are still in the development phase and are not yet commercially available.

II. Contribution

This article improves and extends the findings from [1], which presents a volume comparison of the passive components of the inverter side of CSC and VSC (current-source-inverter CSI and voltage-source-inverter VSI). There, in the first step, analytic relationships for the design of the components were derived. Then, based on the determined quantities, the volume of the passive components of a CSI and a VSI with a sinusoidal output filter is calculated, which can provide a three-phase line-to-line output voltage of 400 V at an output current of 10.6 A (7.3 kW).

In this article, the design process of the passive components of the CSI is explained in more detail and more general relationships between the basic design parameters like the maximum output voltage or current and the passive component volume are derived. For this purpose, the analytic design of the passive components is first revisited in Section III where Section III-A describes the underlying space vector modulation (SVM) concept.

As regards the dimensioning of the filter capacitors, a few studies have already been carried out on this subject. [16] provides the basis for calculating the capacitance, but only the harmonic content of the output voltages is derived and no formulae for the capacitaces are given. In [17] and [18], on the other hand, an equation for the filter capacitors is given directly, but there is no derivation and the remaining constraints of the filter capacitors, such as the maximum permissible voltage and RMS current, are not dealt with. Therefore, in Section III-B, a detailed dimensioning process of the filter capacitors is presented, taking into account not only their capacitance but also other constraints.

Several methods have been described in the literature for the design of the DC-link inductor, all of which give similar results. However, [17], [18], [19], [20] each only describe a formula for the inductance of the DC-link inductor, which does not take into account the other constraints of the design such as the RMS current and the maximum current with respect to saturation. In Section III-C, therefore, a detailed derivation of the necessary parameters for the DC-link inductance is presented in order to be able to easily adapt them to newly developed control and modulation schemes.

In Section IV the design and selection process for minimizing volume and occupied board area of the filter capacitors is shown, where, in contrast to [1], the dielectric is considered in greater depth and the parallel and series connection of commercially available components is taken into account. For the physical design of the DC-link inductance in Section V, the method from [1], which is based on [21] is described in further detail. It is extended by a better approximation of the winding geometry and takes into account the additional volume of the outer layers of the winding and adds it to the total volume of the device. In addition, the approximation of losses is improved by better modelling of the inductor current waveform and a wider range of available core materials is considered for optimisation. Section VI recapitulates the obtained results and highlights the relationships of the volume of the respective passive components in relation to various fundamental design parameters (e.g., system power, output voltage harmonic content,...) of the CSI. The results are then summarized in Section VII.

III. Design of the CSI's Passive Components

This section describes the design process for the passive components of the CSI, the DC-link inductor, and the filter capacitors. For this purpose, the space vector modulation strategy for the inverter is first explained, on the basis of which the following calculations are carried out. The parameters required to properly select the filter capacitors include the capacitance of the filter capacitors C_f, the maximum tolerable peak-to-peak value of the capacitor voltage ripple $\Delta v_{\mathrm{C\,max}}$, the maximum RMS current $I_{\mathrm{C\,max}}$ through and the maximum occurring voltage across the filter capacitors $v_{\mathrm{C\,max}}$. For the DC-link inductor, the parameters are the inductance of the DC-link inductor L_dc, the maximum tolerable peak-to-peak value of the inductor current ripple $\Delta i_{\mathrm{dc\,max}}$ as well as the maximum inductor RMS current $I_{\mathrm{dc\,max}}$ and, regarding saturation, the peak value of the current $i_{\mathrm{dc\,max}}$.

A. Space Vector Modulation

Fig. 1 portrays the simplified circuit model of the CSI circuit. The rectifier on the input side is replaced by a controllable voltage source since this publication only covers the inverter part of the circuit, which consists of a rectifier stage as well. It is assumed that in steady-state operation this voltage source always outputs the voltage v_dc necessary to keep the average value of the DC-link current $\bar{i}_\mathrm{dc}$ at the value selected in the design process. The semiconductor switches are modeled by ideal reverse-blocking switches. The filter capacitors C_f placed between the load and the outputs of the semiconductor stage are responsible for providing an alternative current path in case of an inductive load where overvoltages would occur if the current

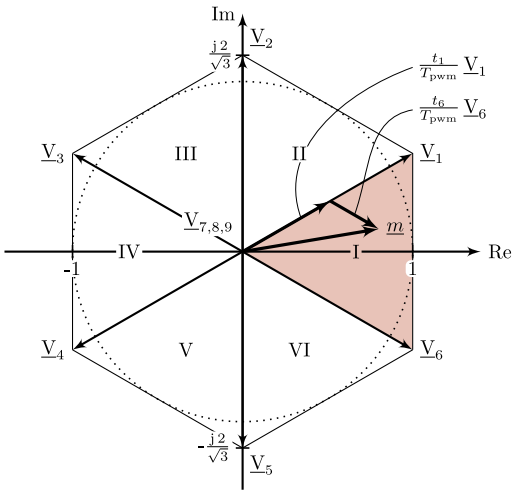

Fig. 3. Space vector diagram for the CSI with 6 active ($\underline{V}_1$...$\underline{V}_6$) and three zero space vectors ($\underline{V}_7$...$\underline{V}_9$) dividing the complex plane into a hexagon with six sectors (I...VI). Here, the reference space vector $\underline{m}$ is located in sector I.

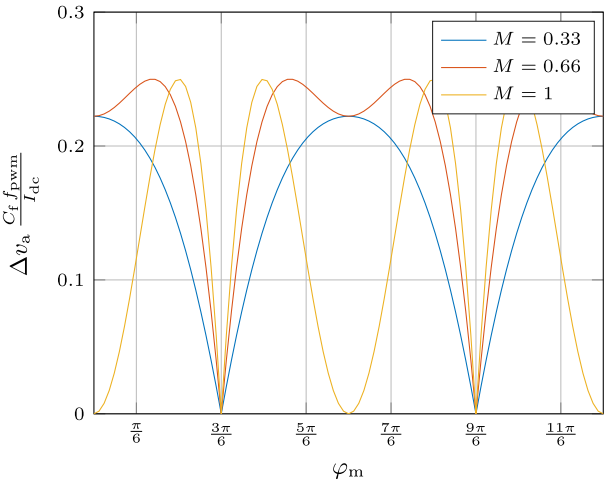

Fig. 4. Normalized peak-to-peak value of the output voltage ripple of *phase a* at different modulating indices M. A maximum of $\Delta v_{\mathrm{a}} \frac{C_{\mathrm{f}}\, f_{\mathrm{pwm}}}{I_{\mathrm{dc}}} = 0.25$ appears for $M \geq \frac{1}{2}$.

carrying DC-link inductor is connected in series to the load at any switching transition.

In the model presented herein, it is assumed that the states of the switches S_1 to S_6 are calculated via sinusoidal space vector modulation with modulation strategy "Mod 1" according to [16]. This strategy offers the lowest switching losses of all strategies with constant DC-link current, because only three commutation processes are carried out per PWM period. The corresponding space vector diagram with the active space vectors $\underline{V}_1$ to $\underline{V}_6$ and the zero states $\underline{V}_7$ to $\underline{V}_9$ in complex vector representation is shown in Fig. 3. Assuming a constant DC-link current $I_{\mathrm{dc}} = \overline{i}_{\mathrm{dc}}$, the three-phase current flowing from the switch nodes can be calculated in complex vector representation $\underline{i}_{\mathrm{S}}$ for the respective switching state by multiplying this DC-link current by one of the specified vectors.

To output an arbitrary complex space vector $\underline{m} = M \cdot \mathrm{e}^{\mathrm{j}\,\varphi_{\mathrm{m}}}$ with maximum length $M_{\mathrm{max}} = 1$, first the sector (I ...VI) in which $\underline{m}$ is located is determined. Subsequently, within a constant time period $T_{\mathrm{pwm}} = \frac{1}{f_{\mathrm{pwm}}}$, the adjacent space vectors bounding the computed sector, as well as an arbitrarily selectable zero space vector, are applied in a time-weighted way (linearly-combined). In contrast to the VSI, the choice of the zero space vector does not influence the voltage or current ripple in the filter capacitors and the DC-link inductance [16]. However, it is possible to optimize the number of switching actions per period through proper selection. The three space vectors, as well as the time intervals with which these are weighted, are specified after the determination of the sector with $\underline{V}_x$ and t_x (adjacent space vector in counterclockwise direction) with $\underline{V}_y$ and t_y (adjacent space vector in clockwise direction) and with $\underline{V}_0$ and t_0 (arbitrary zero space vector). For example, if $\underline{m}$ is located in sector I, $\underline{V}_x = \underline{V}_1$, and $\underline{V}_y = \underline{V}_6$. The time intervals for the weighting can then be calculated by (1).

$$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \frac{1}{f_{\mathrm{pwm}}} \cdot \begin{bmatrix} \Re\mathfrak{e}(\underline{V}_x) & \Im\mathfrak{m}(\underline{V}_x) \\ \Re\mathfrak{e}(\underline{V}_y) & \Im\mathfrak{m}(\underline{V}_y) \end{bmatrix}^{-1} \cdot \begin{bmatrix} \Re\mathfrak{e}(\underline{m}) \\ \Im\mathfrak{m}(\underline{m}) \end{bmatrix} \tag{1}$$

B. Parameters of the Filter Capacitors

Assuming that the complex load current space vector $\underline{i}$ is constant over the time duration of a switching period, the current into the filter capacitors $\underline{i}_{\mathrm{C}}$ can be calculated via the corresponding KCL, $\underline{i}_{\mathrm{C}} = \underline{i}_{\mathrm{S}} - \underline{i}$, for one time interval where the switch position does not change.

It is assumed that the load current space vector corresponds to the average value of the output current over the course of a switching period, $\underline{i} = \underline{m} \cdot I_{\mathrm{dc}}$. The change in the output voltage space vector $\underline{v}$ during a time interval can then be calculated by substituting the capacitor current into the component equation for the capacitor. The resulting transformed difference equations are shown in (2) for the respective time intervals.

$$\begin{bmatrix} \Delta\underline{v}_x \\ \Delta\underline{v}_y \\ \Delta\underline{v}_0 \end{bmatrix} = \frac{I_{\mathrm{dc}}}{C_{\mathrm{f}}} \cdot \begin{bmatrix} (\underline{V}_x - \underline{m}) \cdot t_x \\ (\underline{V}_y - \underline{m}) \cdot t_y \\ -\underline{m} \cdot t_0 \end{bmatrix} \tag{2}$$

This equation can then be further evaluated for each sector and, to obtain the change in phase voltage, be transformed back from the complex space vector representation to phase quantities. To compute the output voltage's peak-to-peak value in *phase a*, Δv_{a}, the resulting equations are analyzed. Δv_{a} can therefore be calculated independently of the sector via (3) [16].

$$\Delta v_{\mathrm{a}} = \frac{I_{\mathrm{dc}}}{C_{\mathrm{f}}\, f_{\mathrm{pwm}}} \left(M\, |\cos(\varphi_{\mathrm{m}})| - M^2\, \cos^2(\varphi_{\mathrm{m}}) \right) \tag{3}$$

Fig. 4 shows the analytically calculated value for $\Delta v_{\mathrm{a}}(\varphi_{\mathrm{m}})$ for different values of M while Fig. 5 shows one period of the simulated output voltage waveform of *phase a* v_{a}. The simulation was performed in *MATLAB/Simulink*, assuming ideal switches for the semiconductor devices. The average DC-link current was chosen to be $\overline{i}_{\mathrm{dc}} = 15\,\mathrm{A}$, the modulation index was $M = 1$, the PWM switching frequency $f_{\mathrm{pwm}} = 100\,\mathrm{kHz}$, the filter capacitances $C_{\mathrm{f}} = 1\,\mu\mathrm{F}$ and the ohmic load was set to provide a line-to-line output voltage of 400 V at this operating

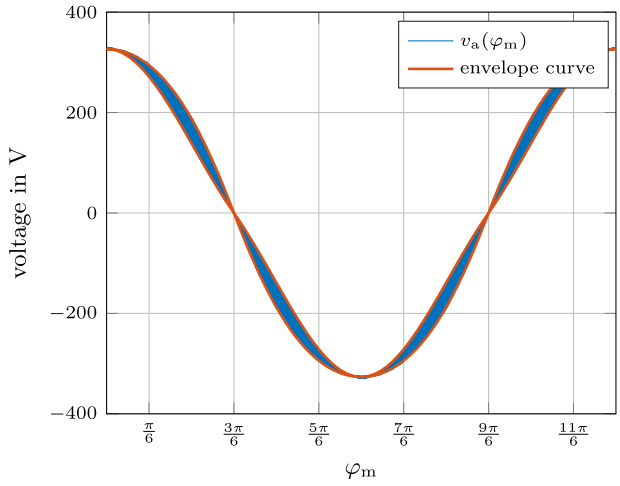

Fig. 5. One period of the simulated sinusoidal inverter output voltage of *phase a*. The envelope curve represents analytically computed values from (3).

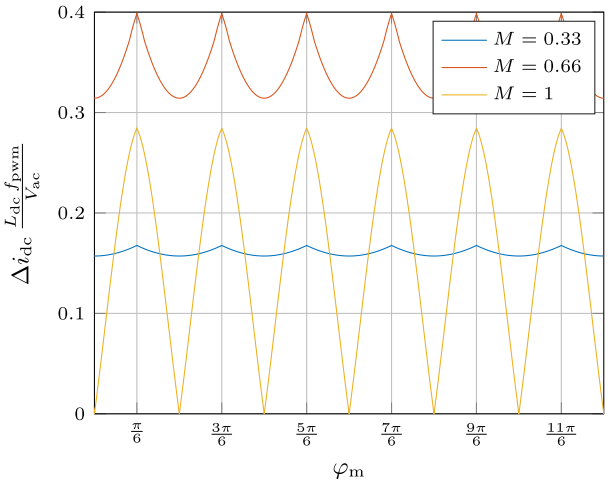

Fig. 6. Normalized peak-to-peak value of the DC-link current for a load power factor $\cos(\varphi_v) = 1$ at different modulating indices M. A maximum of $\Delta i_{dc} \frac{L_{dc} f_{pwm}}{V_{ac}} = \frac{8\sqrt{2}}{27}$ appears at $M = \frac{4}{3\sqrt{3}}$.

point. The additional envelope curve plotted in Fig. 5 was calculated analytically using (2). It can be observed that the analytical computation of the voltage ripple agrees excellently with the simulated values. Any deviations are due to the ripple of the DC-link current, which is neglected in the analytic derivation.

To obtain a correlation for the choice of filter capacitors based on the maximum tolerable output voltage ripple Δv_{max}, (2) is analyzed and converted to C_f.

$$C_f = \frac{I_{dc}}{4\,\Delta v_{max}\,f_{pwm}} \tag{4}$$

It should be noted, that Δv_{max} is independent of the power factor of the load and can be found at $M \in [\frac{1}{2}, 1]$.

Additionally, with the help of the presented derivations, the maximum voltage occurring at the capacitors $v_{C\,max}$ can also be estimated. This occurs when the peak value of the voltage ripple and, due to a power factor $\cos(\varphi) \neq 1$ of the load, the peak value of the fundamental wave coincide. $v_{C\,max}$ can be computed using (5).

$$v_{C\,max} = \sqrt{2}\,V_{ac} + \frac{\Delta v_{max}}{2} \tag{5}$$

To compute the RMS current through each of the filter capacitors I_C during operation, the RMS value of the sinusoidal output current I is subtracted quadratically from the RMS current at the switch nodes I_S given in [16] resulting in (6). The maximum value $I_{C\,max}$ appears at $M = \frac{2}{\pi}$ and can be computed by (7).

$$I_C = I_{dc} \cdot \sqrt{\frac{2\,M}{\pi} - \frac{M^2}{2}} \tag{6}$$

$$I_{C\,max} = I_{dc} \cdot \frac{\sqrt{2}}{\pi} \tag{7}$$

C. Parameters of the DC-Link Inductor

The peak-to-peak value of the DC-link current Δi_{dc} is calculated in a similar way. It is now assumed that instead of i_{dc} the circuit's complex output voltage $\underline{v} = \sqrt{2}\,M\,V_{ac}\,e^{j\varphi_v}$ is constant during one switching period. Here, V_{ac} describes the maximum RMS value of the phase voltages at the inverter output (occurs at $M = 1$ but is load dependent) and φ_v the phase shift between the fundamental waveform of output current (reference signal) and output voltage. The DC-voltage source modeling the rectifier must therefore provide the voltage $v_{dc} = \frac{3}{\sqrt{2}}\,M^2\,V_{ac}\,\cos(\varphi_v)$ to maintain the circuit's power balance in steady-state operation and thus keep the average value of the DC-link current constant. For the following calculation, the output voltage $\underline{v}$ can no longer be considered a complex vector and has to be split into it's three-phase fundamental waveform components.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = M\,\sqrt{2}\,V_{ac}\,\cos\left(\varphi_m + \varphi_v + \begin{bmatrix} 0 \\ \frac{2\pi}{3} \\ -\frac{2\pi}{3} \end{bmatrix}\right) \tag{8}$$

In addition, the switch positions of S_1 to S_6 have to be taken into account. Using the time intervals calculated by (1) for a reference space vector in sector I, t_{xI}, t_{yI} and, t_{0I}, the change in current during each interval through the DC-link inductance can be computed using the difference equation shown in (9).

$$\begin{bmatrix} \Delta i_{dc\,xI} \\ \Delta i_{dc\,yI} \\ \Delta i_{dc\,0I} \end{bmatrix} = \frac{1}{L_{dc}} \cdot \begin{bmatrix} (v_{dc} - v_a + v_c) \cdot t_{xI} \\ (v_{dc} - v_a + v_b) \cdot t_{yI} \\ v_{dc} \cdot t_{0I} \end{bmatrix} \tag{9}$$

The peak-to-peak value of the DC-link current Δi_{dc} is the maximum value of the current change of the three intervals and depends on the parameters φ_{vi}, φ_m, and M. Further evaluation of (9) for all sectors reveals that Δi_{dc} is periodic with respect to $\frac{\pi}{3}$. Fig. 6 shows the analytically calculated value for $\Delta i_{dc}(\varphi_m)$ for different values of M and $\cos(\varphi_v) = 1$. The analytic derivations were again verified in a simulation with ideal semiconductor switches in *MATLAB/Simulink*. The basic simulation parameters were selected to be the same as in Section III-B. Fig. 7 shows the simulated waveform of the DC-link current i_{dc} over one period of the output currents along with the analytically derived enveloping curve calculated using (9). The analytic computation

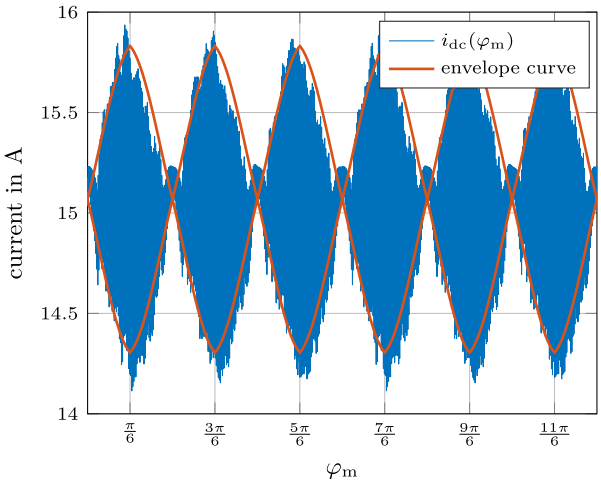

Fig. 7. DC-link current over one period of the simulated sinusoidal inverter output. The envelope curve represents analytically computed values from (9).

of the current ripple shows good agreement with the simulated values. Occurring deviations are due to the ripple of the output voltage, which is neglected in the analytic derivation.

The maximum value of the current ripple $\Delta i_{\mathrm{dc\,max}}$ for $\cos(\varphi_v) = 1$, can be calculated by analyzing (9) which, by transforming, yields an estimation formula for L_{dc}. It occurs at $M = \frac{4}{3\sqrt{3}}$.

$$L_{\mathrm{dc}} = \frac{V_{\mathrm{ac}}}{\Delta i_{\mathrm{dc\,max}}\, f_{\mathrm{pwm}}} \cdot \frac{8\sqrt{2}}{27} \tag{10}$$

Although Δi_{dc} can become larger than the value given in (10) for $\cos(\varphi_v) < 1$, this only happens from about $\cos(\varphi_v) \approx 0.83$. The results of the derived calculation method correspond to the methods often found in the literature [18], [20].

Regarding the saturation of the DC-link inductance, based on the (10) transformed to $\Delta i_{\mathrm{dc\,max}}$, the maximum current through the DC-link inductance $i_{\mathrm{dc\,max}}$ can be calculated by (11) by addition to the mean value of the DC-link current $\bar{i}_{\mathrm{dc}}$.

$$i_{\mathrm{dc\,max}} = \bar{i}_{\mathrm{dc}} + \frac{\Delta i_{\mathrm{dc\,max}}}{2} \tag{11}$$

The RMS value of the DC-link current I_{dc} necessary for estimating the copper losses in the inductance can only be calculated approximately. It is composed of the constant average DC-link current $\bar{i}_{\mathrm{dc}}$ and the AC component $\widetilde{i}_{\mathrm{dc}}$. As a simplification, it is assumed that $\widetilde{i}_{\mathrm{dc}}$ has a pure triangular shape. It can therefore be obtained from the peak value of (9) and the crest factor $\sqrt{3}$ for triangular signals in (12).

$$\widetilde{i}_{\mathrm{dc}} \approx \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{\Delta i_{\mathrm{dc}}}{2\sqrt{3}}\right)^2 d\varphi_m} \tag{12}$$

The equation was evaluated numerically for unity power factor $\cos\varphi_v = 1$. Here, the maximum AC component occurs at about $M \approx 0.7$ and can be calculated by

$$\widetilde{i}_{\mathrm{dc\,max}} \approx \Delta i_{\mathrm{dc\,max}} \cdot 0.239. \tag{13}$$

Thus, the maximum RMS value of the DC-link current $I_{\mathrm{dc\,max}}$ can be estimated by (14).

$$I_{\mathrm{dc\,max}} \approx \sqrt{\bar{i}_{\mathrm{dc}}^2 + \widetilde{i}_{\mathrm{dc\,max}}^2} \tag{14}$$

To determine the volume and the occupied board area of the passive components of the current-source inverter topology, the derived design parameters presented in the previous two sections were used. The volume for filter capacitors is estimated by selecting suitable components available on the market and optimizing their volume and board area respectively. The DC-link inductance design is based on a method presented in the literature [21], which aims to optimize the volume and losses of DC-link inductances for CSIs. The optimization results for both the filter capacitors and the DC-link inductor are then analytically interpolated to obtain empirical estimation formulas for further optimization steps.

IV. Design of the Filter Capacitors

For the determination of board area and volume of the filter capacitors a database was created from the available components of the manufacturers Murata [22], TDK [23] and KEMET [24]. Surface mountable multi-layer ceramic capacitors (MLCCs) utilizing the Class I dielectric C0G (NP0) according to standard EIA-198-1-F-2002 were considered for selection. Capacitors based on this dielectric offer excellent temperature stability, low ESR and good DC bias performance at the cost of lower capacitance per volume at a certain rated voltage. The extremely low ESR of MLCCs based on these dielectric materials results in negligible losses in these devices. Therefore, many manufacturers do not specify concrete values for the maximum permissible ripple current. In most cases, only the ESR over the frequency is specified. For instance, the one of the eight parallel volume optimised MLCCs from the following design example in Section IV-A has an ESR of 2.74 $\mathrm{m\Omega}$ at a frequency of 100 kHz, resulting in dielectric losses of approximately 2 mW per capacitor at the computed maximum RMS current flowing through them. Ceramic capacitors with higher class, ferroelectric dielectrics such as X7R or X5R should not be used for applications in CSIs, as these are usually only specified for DC voltages and feature considerably higher losses. Nevertheless, even when designing with MLCCs with Class I dielectrics, the expected losses should be checked after component selection.

The volume per capacitance and the PCB area required per capacitance were then optimised using the database built up by the aforementioned manufacturers. Parallel connection of several capacitors to increase the capacitance and series connection to increase the maximum voltage were also taken into account. The area and volume calculations for both single and multiple components considered the minimum tolerable distances between components according to IPC-7351 Density Level C: Minimum (Least) Land Protrusion.

For the estimation of optimal volume and board area per capacitance of a configuration consisting of a number of individual capacitors, a maximum tolerable rated voltage $V_{\mathrm{r\,ref}}$ is defined in the first step. Only capacitor configurations with an actual rated voltage $V_{\mathrm{r}} > V_{\mathrm{r\,ref}}$ are considered for further optimization. From

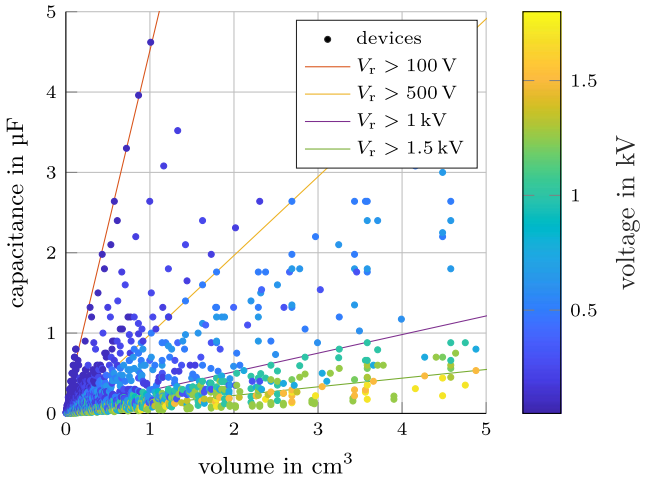

Fig. 8. Graphical visualization of the optimization process for the volume of the filter capacitors. Each dot represents a capacitor arrangement that can be single parts or a combination of series and parallel connection of several components with a total rated voltage $V_r > 100\,V$. Besides the linearized configuration with highest capacitance per volume for $V_r > 100\,V$ the fronts for several different higher voltages are depicted as well.

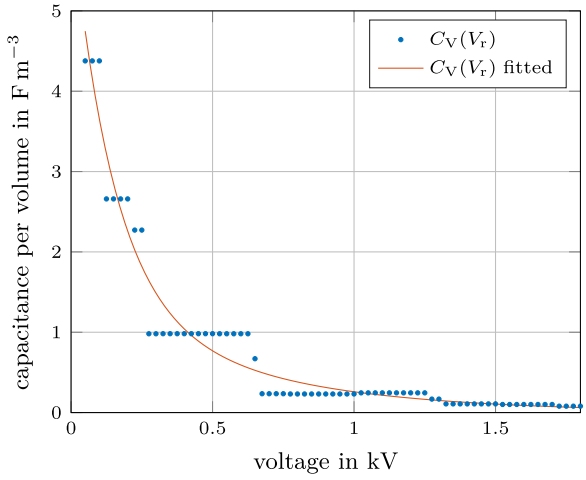

Fig. 9. Volume optimized capacitance per volume of the selected filter capacitors plotted against the rated voltage. The values obtained were interpolated with a two-term exponential model to obtain an analytical relationship.

these configurations, those with the smallest volume or board area per capacitance are determined. Since these relationships are approximately linear, the determined component values can be interpolated with a straight line. Thus, for a selected voltage $V_{r\,ref}$, an optimum relative capacitance per volume C_V (relative capacitance in Fm^{-3}) or board area C_A (relative capacitance in Fm^{-2}) can be specified representing these straight lines. Fig. 8 shows a graphical visualization of this process for the volume of filter capacitors. A point corresponds to a capacitor configuration consisting of one or more individual components connected in parallel or in series, all of which have a rated voltage $V_r > 100\,V$. The capacitance of each configuration is plotted over the volume and the color coding symbolizes V_r. The straight lines approximate the points with largest capacitance per volume of a certain V_r.

This procedure was then performed several times for $V_{r\,ref}$ between 50 V and 1.8 kV in 25 V steps. The results of all calculations for relative capacitance per volume C_V is shown in Fig. 9. A point there represents the slope of one of the determined straight lines. From this diagram, a general relationship between capacitance per volume and rated voltage can then be read for available MLCCs with Class I dielectric. Fig. 9 shows this curve for volume per capacitance obtained from the optimization. The discrete levels arise from the fact that the rated voltage of the individual components is sometimes only available in rough steps (e.g. 100 V, 250 V, 350 V, ...).

Both this relationship and the relationship for the occupied board area are then fitted with the two-term exponential model shown in (15).

$$C_V = a\,e^{b\,V_r} + c\,e^{d\,V_r} \tag{15}$$

The relative capacitance per board area C_A can also be determined using (15). The parameters of both fit models can be read from table Table I.

TABLE I
PARAMETERS OF THE TWO-TERM EXPONENTIAL MODELS FOR THE ANALYTIC VOLUME AND AREA FIT

	a	b	c	d
volume fit	4.79	$-6.80 \cdot 10^{-3}$	1.46	$-1.75 \cdot 10^{-3}$
area fit	$1.96 \cdot 10^{-2}$	$-2.43 \cdot 10^{-3}$	$1.88 \cdot 10^{-5}$	$1.69 \cdot 10^{-3}$

Using these two models and the associated parameters, a power electronics design engineer can make a simple estimate of the approximate volume or board area required for the filter capacitors of a CSI without having to perform a complicated optimization.

A. Filter Capacitor Design Example

To make things clearer, a short design example is carried out. The filter capacitors of a CSI with an output power of $P_{ac} = 5\,kW$ at a line-to-line RMS output voltage of $V_{ac\,ll} = 400\,V$ ($V_{ac} = 231\,V$) are to be designed. The peak value of the output current and thus the necessary DC-link current in this case corresponds to $I_{dc} = \frac{\sqrt{2}\,P_{ac}}{\sqrt{3}\,V_{ac\,ll}} = 10.2\,A$. The PWM switching frequency is $f_{pwm} = 100\,kHz$ and the maximum tolerable voltage ripple is set as $\Delta v_{max} = 5\%\,V_{ac}\,\sqrt{2} = 32.7\,V$.

By using (4), (5) and (7), the filter capacitance $C_f = 1.56\,\mu F$, the peak value of the voltage $v_{C\,max} = 343\,V$ at and the RMS current through the filter capacitance $I_{C\,max} = 5.59\,A$ can be calculated.

Using (15) and the parameters from Table I and a safety factor for the maximum capacitor voltage of 30%, the optimal volume can now be estimated with $V_{est} = \frac{C_f}{C_V(1.3\,v_{C\,max})} = 1.74\ cm^3$ or the optimal consumed board area can be estimated with $A_{est} = \frac{C_f}{C_A(1.3\,v_{C\,max})} = 2.34\ cm^2$. For this case, the volume optimal capacitor configuration with 8 parallel connected components of type *C2220C204KCGLCAUTO* has a volume of 1.51 cm^3 and the board area optimal capacitor configuration with 2 parallel connected components of type *CKC33C884KCGLC7805* has an

area of 2.16 cm^2. The small deviations between these and the estimated values are due to the large steps between the available rated voltage values.

V. Design of the DC-Link Inductor

The calculation for volume and the required board area of the DC-link inductor is based loosely, as already shown in [1], on the method demonstrated in [21]. However, in the present publication, major improvements have been made to this. Here, the optimization is performed directly with commercially available torroidal core geometries and their data. The most important geometrical parameters for the inductance determination, the mean magnetic path length and the cross-sectional area of the torroid, are taken directly from the manufacturer. Furthermore, the relative permeability $\mu_\mathrm{r}(H)$ provided by the manufacturer is used directly instead of the analytically fitted equation for $B(H)$ to account for the saturation behavior of the cores. In addition, in the present optimization the determination of the copper losses and the actual volume of the inductors is greatly improved and the optimization is performed for a wider range of materials with different relative permeabilities. Finally, as for the filter capacitors, a general prediction method is presented to determine the optimum volume or board area with respect to the required inductance and DC-link current.

In the design method presented, an attempt is made to minimize the volume or board area and total losses consisting of core losses and copper losses. For the cores used, toroidal powder cores with molypermalloy (MPP) material from the manufacturer *Magnetics* are investigated. This manufacturer provides analytic fit equations for the $B(H)$ curve and differential relative permeability $\mu_\mathrm{r}(H)$ curve, as well as the Steinmetz parameters K_c, α and β for the offered materials and cores [25]. The geometrical parameters of toroidal cores are given in the form of outer diameter D_c, inner diameter d_c, height h_c, core volume V_c, core cross-sectional area A_c and mean magnetic path length l_c. The design process is performed numerically for each available core geometry (the outer diameters range from 4.19 mm to 167.21 mm) with each available material featuring a nominal relative permeability between 14 and 550. The initial parameters for the optimization are the desired values for the inductance L, the PWM frequency f_pwm, the average DC-link current $\bar{i}_\mathrm{dc}$ and the RMS value of the AC component of the DC-link current $\widetilde{i}_\mathrm{dc\,max}$ known from the design process.

A. Determination of the Number of Turns

At the beginning of the optimization, a core geometry with a nominal relative permeability is selected from the manufacturer's data. Then, the number of turns N around the core is increased stepwise and the mean magnetic field strength $\overline{H}$ is calculated by (16) at each increment.

$$\overline{H} = N \cdot \frac{\bar{i}_\mathrm{dc}}{l_\mathrm{c}} \tag{16}$$

Here, $\bar{i}_\mathrm{dc}$ is the expected average DC-link current through the inductor. In each step, the inductance L for the given number of windings can then be calculated using (17).

$$L = \frac{N^2\, A_\mathrm{c}}{l_\mathrm{c}} \cdot \mu_\mathrm{r}\left(\overline{H}\right), \tag{17}$$

Here, $\mu_\mathrm{r}(\overline{H})$ is determined via the analytic relationship specified by the manufacturer. The process of stepwise increase of N is performed until L is larger than the desired inductance. If the number of turns calculated would lead to too much saturation (e.g. if $\mu_\mathrm{r}(\overline{H})$ deviates too much from the nominal value), the core format used is already discarded after this step because the desired inductance can not be realised.

B. Determination of the Core Losses

After determining the number of turns, the core losses can be estimated using the Steinmetz parameters provided by the manufacturer. For this purpose, it is assumed that on average the largest core losses occur when the AC component of the DC-link current has the largest RMS value. This occurs, as already mentioned in Section III-C for $M \approx 0.7$, and can be calculated using (13). For a simple estimation, the calculated RMS value $\widetilde{i}_\mathrm{dc\,max}$ is then doubled and multiplied by the factor $\sqrt{3}$ for triangular signals to obtain the peak-to-peak value of an equivalent triangular signal. from this, similar to (16), a field strength ripple ΔH is calculated, which is superimposed on the constant mean field strength. Assuming that $\Delta H << \overline{H}$, the flux density of the B-H curve changes little in the area of the ripple and can therefore be assumed to be linear in that range with slope $\mu_\mathrm{r}(\overline{H})$. The ripple of the magnetic flux density ΔB can then be calculated by (18).

$$\Delta B \approx \mu_\mathrm{r}\left(\overline{H}\right) \cdot \Delta H = \mu_\mathrm{r}\left(\overline{H}\right) \cdot N \cdot \frac{2\sqrt{3}\,\widetilde{i}_\mathrm{dc\,max}}{l_\mathrm{c}} \tag{18}$$

If ΔB is now substituted into the Steinmetz equation in (19), the maximum core losses occurring during the operation of the converter can be estimated.

$$P_\mathrm{c} \approx K_\mathrm{c} \cdot \left(\frac{f_\mathrm{pwm}}{1000}\right)^{\alpha} \cdot \left(\frac{\Delta B}{2}\right)^{\beta} \cdot (1000\, V_\mathrm{c}) \tag{19}$$

The two factors of 1000 each come from the fact that in the Steinmetz equation the frequency is put in kHz, and the relative power dissipation per volume is put in $\mathrm{mW cm^{-3}}$.

C. Determination of the Copper Losses

For the calculation of the copper losses as well as the total volume of the wound inductor, a method is used which is based on the actual winding process and does not use filling factors as in [21]. Therefore, a wire diameter is selected from a set of diameters (AWG 1 to 50). This wire is then iteratively wound onto the core by an algorithm starting with the first layer. If the desired number of turns can not be achieved by winding one layer another one is applied. The inner diameter of the inductor (window area) for the application of a new layer decreases with the number of layers. The possible number of turns of the kth

layer, $N_{k\,\max}$ can be calculated with (20).

$$N_{k\,\max} = \frac{\pi}{\arcsin\left(\frac{R_\mathrm{w}}{r-(2\,k-1)\,R_\mathrm{w}}\right)} \tag{20}$$

Here, $R_\mathrm{w} = \frac{D_\mathrm{w}}{2}$ is the wire radius and $r = \frac{d}{2}$ represents the core inner radius. In this model, it is assumed that one layer reduces the usable inner radius of the core window area by D_w and that the outer diameter and the height of the total wound coil increase by $2\,D_\mathrm{w}$ per layer. If the inner usable diameter of the core respectively the window area is reduced to zero by selecting a wire that is too thick, the desired number of turns cannot be realized with this diameter, and the process is aborted and started with the next wire from the set.

The length of the wire increases per wound layer k by the number of windings applied ($N_k = N_{k\,\max}$ for a full layer, potentially less in the last layer K) and can be calculated by

$$l_k = N_k \cdot (D - d + 2\,h + 8\,(2\,k-1)\,R_\mathrm{w})\,. \tag{21}$$

The total wire length l_w is the sum of the calculated lengths of the individual layers ($l_\mathrm{w} = \sum_{k=1}^{K} l_k$).

The volume V_L occupied board area A_L (horizontal position) and inductor surface area A_s (for estimation of the inductor heating) of the inductor can then be calculated using the core outer dimensions increased by the winding according to (22).

$$\begin{aligned} V_\mathrm{L} &= \pi\,(R + k\,D_\mathrm{w})^2 \cdot (h + 2\,k\,D_\mathrm{w}) \\ A_\mathrm{L} &= \pi\,(R + k\,D_\mathrm{w})^2 \\ A_\mathrm{s} &= 2\pi\,\left(R^2 - r^2 + 2\,k\,D_\mathrm{w}\,(R+r)\right) \\ &\quad + 2\pi\,(h + 2\,k\,D_\mathrm{w}) \cdot (r + R) \end{aligned} \tag{22}$$

After determining the wire length and the number of layers, the DC resistance $\overline{R}$ of the winding can be calculated through

$$\overline{R} = \rho_\mathrm{cu} \cdot \frac{l_\mathrm{w}}{R_\mathrm{w}^2\,\pi}, \tag{23}$$

where the specific resistivity of copper ρ_cu is assumed to be $0.0178\,\Omega\mathrm{mm}^2\mathrm{m}^{-1}$. For the calculation of AC resistance $\widetilde{R}$, which occurs due to skin and proximity effect, the method from [26], [27] is applied as described in [21]. Equation (24) shows the relationship for the computation of the AC resistance $\widetilde{R}_n$ for each harmonic order n of the AC current.

$$\begin{aligned} \widetilde{R}_n = \overline{R}\,\frac{\gamma}{2}\Bigg[& \frac{\mathrm{ber}\,\gamma\,\mathrm{bei}'\,\gamma - \mathrm{bei}\,\gamma\,\mathrm{ber}'\,\gamma}{\mathrm{ber}'^2\gamma + \mathrm{bei}'^2\gamma} \\ & - 2\pi\,\eta^2\,\frac{4\,K-1}{3}\,\frac{\mathrm{ber}_2\gamma\,\mathrm{ber}'\gamma + \mathrm{bei}_2\gamma\,\mathrm{bei}'\gamma}{\mathrm{ber}^2\gamma + \mathrm{bei}^2\gamma}\Bigg] \end{aligned} \tag{24}$$

where

$$\begin{aligned} \delta &= \frac{1}{\sqrt{\pi\,n\,f_\mathrm{pwm}\,\mu_0\,\frac{1}{\rho_\mathrm{cu}}}} \\ \eta &= \frac{D_\mathrm{w}}{t}\,\sqrt{\frac{\pi}{4}} \\ \gamma &= \frac{D_\mathrm{w}}{\delta\,\sqrt{2}} \end{aligned} \tag{25}$$

with the parameters:

- δ: skin depth
- η: porosity factor
- D_w: wire diameter
- n: harmonic order
- f_pwm: PWM frequency (fundamental frequency triangular waveform)
- ρ_cu: relative conductivity copper
- t: distance between two adjacent conductors (here, $t = D_\mathrm{w}$ was assumed)

The functions "ber" and "bei" represent the Kelvin functions based on the Bessel function of the first kind and order ν, $J_\nu(z)$, where

$$\begin{aligned} \mathrm{ber}_\nu x &= \Re\left\{J_\nu\left(x\,\mathrm{e}^{\frac{3\pi\,i}{4}}\right)\right\} \\ \mathrm{bei}_\nu x &= \Im\left\{J_\nu\left(x\,\mathrm{e}^{\frac{3\pi\,i}{4}}\right)\right\} \end{aligned} \tag{26}$$

For the zero-order Bessel- and Kelvin functions $\nu = 0$ the subscript is not written. The required derivative of the zero-order Kelvin functions can be solved analytically by

$$\begin{aligned} \mathrm{ber}'x &= \frac{\mathrm{bei}_1 x + \mathrm{ber}_1 x}{\sqrt{2}} \\ \mathrm{bei}'x &= \frac{\mathrm{bei}_1 x - \mathrm{ber}_1 x}{\sqrt{2}}. \end{aligned} \tag{27}$$

The AC component of the DC-link current is again assumed to be a simple triangular signal with an RMS value of $\widetilde{i}_{\mathrm{dc}\,\max}$ according to (13). From this, an equivalent amplitude can again be calculated with the factor $\sqrt{3}$. The Fourier coefficients $\widetilde{I}_n$, which are necessary for the calculation of the AC copper losses $\widetilde{P}_\mathrm{cu}$, can therefore be calculated by

$$\widetilde{I}_n = \begin{cases} \sqrt{3}\,\widetilde{i}_{\mathrm{dc}\,\max}\,\frac{8}{\pi^2\,n^2} & \forall\, n \text{ odd} \\ 0 & \forall\, n \text{ even} \end{cases} \tag{28}$$

The estimated AC losses $\widetilde{P}_\mathrm{cu}$, including skin and proximity effect, can then be obtained from the sum of the individual power losses. An equivalent AC resistance $\widetilde{R}$ can be determined by the assumed current RMS value.

$$\begin{aligned} \widetilde{P}_\mathrm{cu} &= \sum_{n=0}^{\infty} \widetilde{R}_n \cdot \widetilde{I}_n \\ \widetilde{R} &= \frac{\widetilde{P}_\mathrm{cu}}{\widetilde{i}^2_{\mathrm{dc}\,\max}} \end{aligned} \tag{29}$$

For practical reasons, the harmonic coefficients are calculated only up to the 9th order, since from this point the harmonic current amplitude is less than 1% of the fundamental amplitude.

Once the copper and core losses are determined, the temperature rise T_{rise} can be calculated as shown in [21] using (30) from [28]. The factor $\frac{1}{10}$ comes from the fact that for this equation in this publication, every power variable is assumed to be in W and the surface area is assumed to be in m^2.

$$T_{\text{rise}} = \left(\frac{P_{\text{c}} + \widetilde{P}_{\text{cu}} + \overline{P}_{\text{cu}}}{10\, A_{\text{s}}} \right)^{0.833} \tag{30}$$

Since the increase of the inductor temperature T from its initial Temperature T_0 affects the specific resistivity of the copper ρ_{cu}, the copper resistances (AC and DC) are adjusted to the elevated temperature according to (31).

$$\overline{R}(T = T_0 + T_{\text{rise}}) = \overline{R}(T = T_0) \cdot (1 + \alpha\, T_{\text{rise}}) \tag{31}$$

The specific temperature coefficient of copper here is $\alpha = 0.00404\ /^{\circ}\mathrm{C}$. Based on the new DC resistance at the elevated temperature, the corresponding new AC and DC copper losses can now be recalculated by (24) and (29) and a resulting temperature rise according to (30) can be determined. This process is continued iteratively until the inductor temperature has reached a steady state. In practice, the number of iterations is limited to four, since the final temperature changes by less than 1% for further iterations [21].

With the consideration of the temperature rise the design of an inductor is completed. From the evaluated parameters, a figure of merit can be obtained for each analyzed core with all determined winding geometries, which is necessary for the calculation of the optimal design. For the optimization of the volume $\mathrm{FOM_V}$ and for the optimization of the board area $\mathrm{FOM_A}$ is given in (32).

$$\begin{aligned} \mathrm{FOM_V} &= V_{\text{L}} \cdot \left(P_{\text{c}} + \widetilde{P}_{\text{cu}} + \overline{P}_{\text{cu}} \right) \\ \mathrm{FOM_A} &= A_{\text{L}} \cdot \left(P_{\text{c}} + \widetilde{P}_{\text{cu}} + \overline{P}_{\text{cu}} \right) \end{aligned} \tag{32}$$

For the selection of the optimized inductance, the inductance with the lowest figure of merit is chosen from the set of generated ones. Fig. 10 shows a graphical visualization of the described design process of the DC-link inductor for optimising its volume. Each point represents an inductor design with its own core geometry and winding configuration for a given set of input parameters. The Red Cross marks the optimal design selected based on the respective figure of merit in (32).

D. Experimental Verification of the Design Process

To verify the demonstrated design process for the inductors, one inductor was practically realised. Measurements were then carried out with this built inductor and its determined parameters were compared with the theoretical values from the design process.

The input parameters for the design of the component included an inductance value of 100 μH at an average current of 5 A, with a current ripple of 1.25 A at a switching frequency of 100 kHz. Based on these specifications, the design process

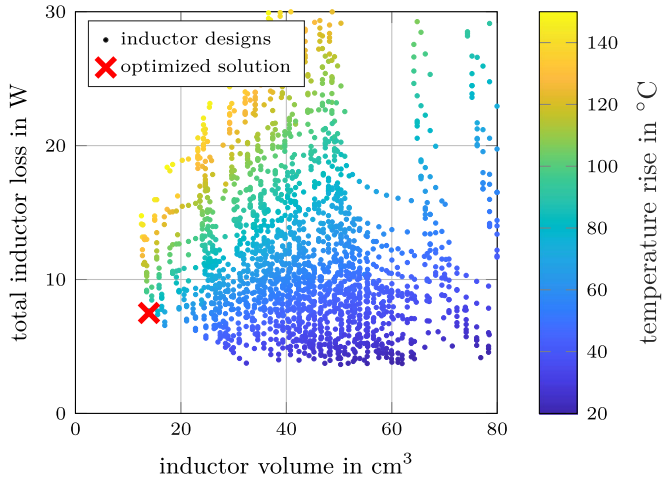

Fig. 10. Graphical visualization of a DC-link inductor design process with input parameters $L = 100\,\mu\mathrm{H}$, $\bar{i}_{\text{dc}} = 10\,\mathrm{A}$, $\widetilde{i}_{\text{dc\,max}} = 1.5\,\mathrm{A}$, $f_{\text{pwm}} = 100\,\mathrm{kHz}$ and $T_{\text{rise}} < 150\,^{\circ}\mathrm{C}$. Each point corresponds to a possible design and is plotted according to the estimated total losses ($P_{\text{c}} + \widetilde{P}_{\text{cu}} + \overline{P}_{\text{cu}}$) and the calculated volume V_{L}. The optimal design determined based on the selected figure of merit is marked with a red cross.

TABLE II
INPUT AND OUTPUT PARAMETERS OF THE DESIGN PROCESS CARRIED OUT FOR A SPECIFIC INDUCTOR

Input Parameters				Output Parameters		
L_{ref}	$\bar{i}_{\text{dc}}$	Δi_{dc}	f_{pwm}	N	D_{w}	core
µH	A	A	kHz	-	mm	-
100	5	1.25	100	38	1.5	*C055894A2*

selected the *C055894A2* core with 38 turns and a wire diameter of 1.5 mm for the component. A summary of the inductance parameters is presented in Table II.

To verify the calculated inductor, it was wound and its parameters were measured and compared with the theoretical values. The inductor was first tested at a selected DC-bias of 5 A. To accomplish this, a square-wave voltage with a duty cycle of 50% and variable amplitude was generated using a half-bridge circuit. The voltage was then fed to the inductor under test via a resistor with a large filter capacitor (2200 μF). The resistors value and the amplitude of the voltage were adjusted until the desired triangular current with an amplitude of 1.25 A and a DC-bias of 5 A was obtained. The capacitor maintained a constant voltage at the resistor, preventing the linear parts of the current waveform from being influenced by the resistor. The basic circuit diagram for this experiment is shown in Fig. 11. The voltage v_{L} and current i measurements for the circuit's inductor were taken at the operating point selected in the design process, as shown in Fig. 12. Both waveforms were captured using an oscilloscope (LeCroy WaveRunner HRO 66Zi).

The expected triangular shape was observed for the current waveform, while the voltage waveform across the inductor appeared rectangular and exhibited almost no DC-bias. Although there was an overshoot at the transitions of the voltage due to the switching behavior of the half-bridge, this did not affect

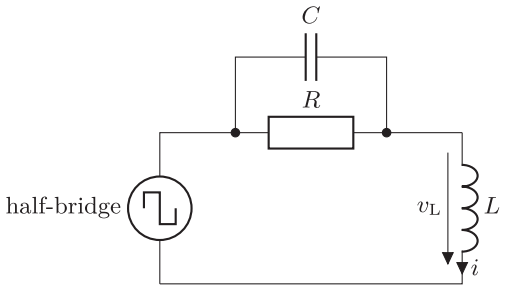

Fig. 11. Basic circuit diagram of the measurement for determining the inductance.

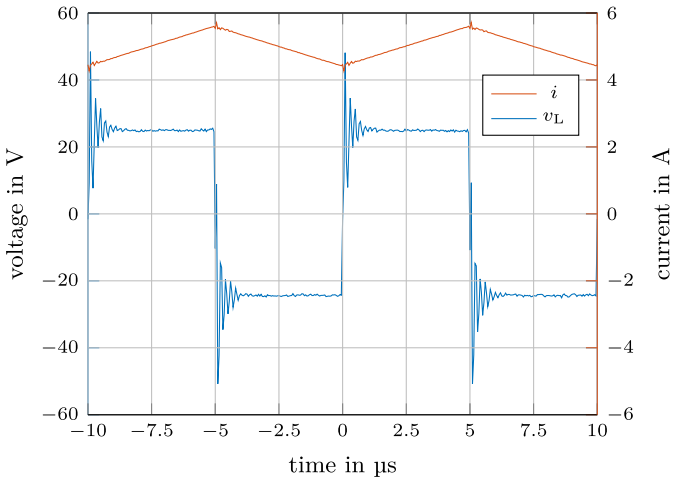

Fig. 12. Two periods of the measured current and voltage waveforms of the circuit from Fig. 11 for the determination of the inductance of the designed inductor.

the measurement. The inductance was determined during time intervals where the voltage remained constant and the current increased linearly, using the equation $L = \frac{\overline{v}_L \Delta t}{\Delta i}$. Here, $\overline{v}_L$ denotes the mean value of the voltage, Δt is the duration, and Δi is the linear change in current over the time period. The measured inductance for the conducted experiment was found to be $L = 105\,\mu\mathrm{H}$. This result is in close agreement with the expected inductance of $100\,\mu\mathrm{H}$.

Measuring the losses occurring in an inductor, such as DC and AC copper losses and core losses, can be challenging due to the reactive power present in the component, which considerably exceeds the active power. In the circuit presented here, reactive power of approximately 125 W is added or removed during half a period, whereas the calculated active losses are only $671\,\mathrm{mW}$. To avoid this problem, we measured only the temperature rise of the inductor in still air and compared it with the value determined during the design process.

We used a thermal camera to capture a thermal image of the inductor after $30\,\mathrm{min}$ of operation at an ambient temperature of $21.5\,^{\circ}\mathrm{C}$, as shown in Fig. 13. The final temperature of the inductor was $34.6\,^{\circ}\mathrm{C}$, corresponding to a temperature increase of $13.1\,^{\circ}\mathrm{C}$. The design process had predicted a temperature rise of $10.4\,^{\circ}\mathrm{C}$, which slightly underestimated the actual measured value.

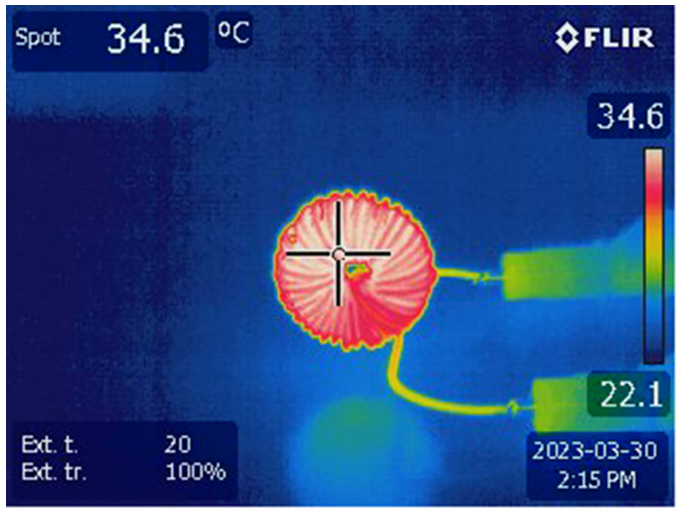

Fig. 13. Thermal image of the built inductor when supplied with a triangular current with an average value of 5 A and a current ripple of 1.25 A. The picture was taken after $30\,\mathrm{minutes}$ when the temperature in still air has reached its steady state.

Based on these results, we conclude that the design process for the inductors is sufficiently accurate and can be used to optimize the inductor in terms of volume and occupied board area.

E. Interpolation of the Inductor Designs

The proposed optimization was now performed for different sets of input parameters (L_{dc}, $\overline{i}_{dc}$, $\widetilde{i}_{dc\,max}$, and f_{pwm}) and the optimal volume or board area was acquired for each inductor. By further analysis of the obtained data, it can be seen that the inductance per volume or board area roughly follows a linear relationship which can be expressed by an inductance per volume L_V (relative inductance in Hm^{-3}) or inductance per board area (relative inductance in Hm^{-2}). The graphical visualization of such an analysis process is shown in Fig. 14 where one dot represents an optimised inductor for a given set of input parameters. The variation of the individual designs is mainly due to the variance of the available core formats. For larger inductance values, fewer formats are available, which results in a greater dispersion of the optimization results.

By linearising the optimized values as inductance per volume or area, similar to the filter capacitors, these values can now be plotted against the average DC-link current $\overline{i}_{dc}$ at a given PWM frequency.

Fig. 15 shows the obtained correlations for the inductance per volume at $f_{pwm} = 50\,\mathrm{kHz}$, $100\,\mathrm{kHz}$ and $200\,\mathrm{kHz}$ and different DC-link currents in the range of $\overline{i}_{dc} = 0.5\,\mathrm{A} \ldots 20\,\mathrm{A}$. These correlations were then fitted with the model from (33), which interpolates the simulated values very well, to obtain an analytical relationship for estimating the volume and required board area.

$$L_V = a \cdot \overline{i}_{dc}^{\,b} + c \tag{33}$$

Table III shows the parameters for the fit equation of the volume and area optimization. For different switching frequencies in the

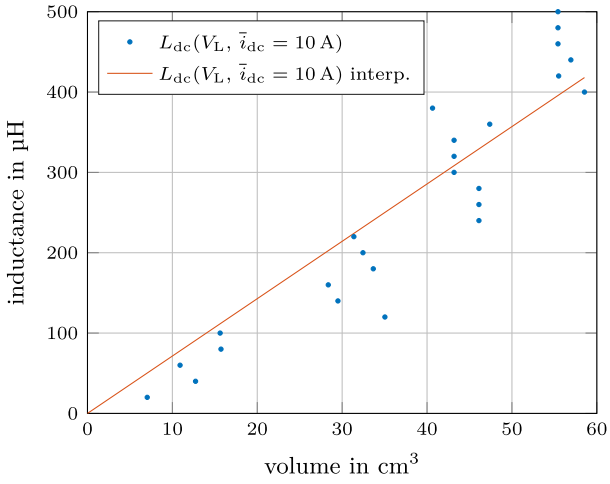

Fig. 14. Optimized set of inductances ($L_{dc} = 20\,\mu H \ldots 500\,\mu H$ in $20\,\mu H$ steps) for an average DC-link current of $\bar{i}_{dc} = 10$ A and a RMS value of the AC component of $\widetilde{i}_{dc} = \frac{25\%\,\bar{i}_{dc}}{\sqrt{3}} = 722$ mA. The values were interpolated with a straight line approximating a constant relationship $\frac{L_{dc}}{V_L}$ for the selected operating point.

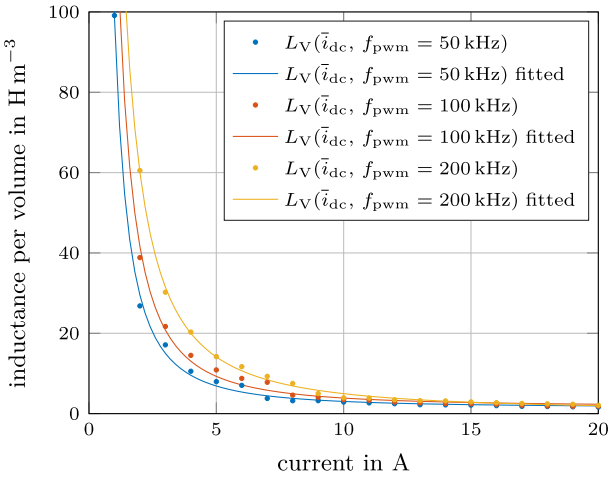

Fig. 15. Interpolation of the determined inductance per volume L_V for different DC-link currents in the range $\bar{i}_{dc} = 0.5$ A ... 20 A and for PWM frequencies of 50 kHz, 150 kHz, and 200 kHz. The RMS value of the AC component of the DC-link current was set to be $\widetilde{i}_{dc} = \frac{25\%\,\bar{i}_{dc}}{\sqrt{3}}$.

range $f_{pwm} = 25\,kHz \ldots 200\,kHz$ (relevant for wide-bandgap material based semiconductor devices).

The calculated values for the selected frequency, DC-link current, and inductance range show that the optimized inductance per volume or unit area decreases sharply, especially for medium DC-link currents $\bar{i}_{dc} < 6$ A, independent of f_{pwm}, and then remains approximately constant for the higher current range. The difference between various selected PWM frequencies is visible (higher switching frequencies lead to an increased volume or area due to the increased core and AC copper losses) but does not have nearly as large an effect as the DC-link current. Using these models and the associated parameters, a simple estimate of the approximate volume or area required for the DC-link inductance can be made, as for the filter capacitors, without having to perform a complicated optimisation.

TABLE III
PARAMETERS OF THE POWER MODELS FOR THE ANALYTIC VOLUME AND AREA FIT

	f_{pwm}	a	b	c
	kHz	-	-	-
volume fit	25	97.6	-1.49	2.01
	50	122	-1.31	0.183
	75	145	-1.30	-0.578
	100	161	-1.32	-0.863
	125	210	-1.53	0.782
	150	256	-1.75	2.36
	175	290	-1.83	2.82
	200	292	-1.82	2.77
area fit	25	0.697	-0.964	0.0415
	50	0.933	-0.969	0.0254
	75	1.04	-0.911	0.0063
	100	1.17	-1.02	0.0211
	125	1.21	-1.10	0.0371
	150	1.31	-1.19	0.0479
	175	1.42	-1.28	0.0595
	200	1.40	-1.16	0.0408

F. DC-Link Inductor Design Example

As for the filter capacitors, a short design example is carried out. The DC-link inductor of a CSI with the same parameters as in the previous example ($P_{ac} = 5$ kW, $V_{ac\,ll} = 400$ V, $I_{dc} = 10.2$ A, $f_{pwm} = 100$ kHz) is to be designed. The the maximum tolerable DC-link current ripple is $\Delta i_{dc\,max} = 25\%\ I_{dc} = 2.55$ A.

By using (17), a DC-link inductance of $L_{dc} = 379\,\mu H$ can be calculated.

Using (33) and the parameters from Table III, the optimal volume can now be estimated by $V_{est} = \frac{L_{dc}}{L_V(\bar{i}_{dc}=10.2\,A)} = 57.3$ cm^3 or the optimal consumed board area can be estimated by $A_{est} = \frac{L_{dc}}{L_A(\bar{i}_{dc}=10.2\,A)} = 29.2$ cm^2 without having to perform a complicated optimization. For this case, the actual volume optimal inductor and the area optimal inductor based on the presented optimisation method have the same core and winding configuration. This is constructed from the core *C055439A2* with a nominal relative permeability of $\mu_r = 60$ having $N = 62$ turns with a wire diameter $D_w = 1.6$ mm. The volume of this inductor is 58.6 cm^3 and the occupied board area in horizontal position is 23.0 cm^2. Both values show good agreement with the estimated results.

VI. SUMMARY OF VOLUME AND BOARD AREA ESTIMATION

From the results obtained in Section IV, it can be seen that the volume and board area of the ceramic capacitors based on the C0G/NP0 dielectric depend in principle only on the rated voltage V_r of the individual components and thus almost only on the maximum RMS output voltage V_{ac}. For power factors of load $\cos(\varphi) \neq 1$, the voltage ripple to (5) must also be taken

into account. Since the optimum volume and board area for a certain rated voltage of the entire structure behave approximately linear to the capacitance, the relationship can be expressed by a capacitance per volume C_{V} or capacitance per area C_{A} which can be determined for the investigated component types according to the empirically determined relationship from (15).

For determining the optimum DC-link inductance, the optimization process in Section V is slightly more complex. However, as for the capacitances, there is an approximately linear relationship between inductance and volume or required board area in the realizable inductance range with the investigated core geometries. This can again be expressed by an inductance per volume L_{V} or area L_{A}, which depend on the DC-link current, the ac component of the DC-link current and the PWM frequency. In the investigations, the maximum AC component of the current was set to 5% of the intermediate circuit current to lock one optimization variable. If this relative inductance is now examined over the average value of the DC-link current, a relationship is found which can be estimated analytically with the power model from (33). The optimal relative inductance changes significantly for small average DC-link currents ($\bar{i}_{\mathrm{dc}} < 6\,\mathrm{A}$) and remains approximately constant for larger currents ($\bar{i}_{\mathrm{dc}} > 10\,\mathrm{A}$). The PWM frequency has little effect on the inductance and is represented by different model parameters.

VII. Conclusion

This article improves in principle the part of [1] which deals with the design of the passive components (filter capacitors and DC-link inductor) of the current-source-inverter topology. For this purpose, first, the space vector modulation necessary for the operation of an inverter as well as the basic analytic correlations required for the design of the components are recapitulated. Based on these relationships, optimal designs for the filter capacitors and DC-link inductor are then determined, taking into account SMD ceramic capacitors with C0G/NP0 dielectric for the capacitors and toroid powder cores with a distributed air gap for the inductor. Both design processes ultimately provide empirical analytical relationships that allow designers of current source converters to quickly estimate component volumes based on a few fundamental design parameters.

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