Fully Passive RF Wake-Up Receiver Including a Small Loop Antenna With −30.7-dBm Sensitivity at 26-kbps Bitrate

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***Abstract*—This brief presents a fully passive RF wake-up receiver (WuRX) fabricated in a 130 nm CMOS process with a matched small loop antenna. The WuRX consists of a high-sensitivity RF energy harvester that supplies the circuitry necessary for passive WuRX functionality. The circuit consists of an on-chip voltage reference, current reference, power-on reset, low-dropout regulator, relaxation oscillator, envelope detector, comparator, and a digital processor. The WuRX supports an input bitrate of 26 kbps and has a user-defined 12-bit wake-up pattern. Measurements at 830 MHz reveal a wake-up sensitivity of −30.7 dBm and a 1 V harvested output sensitivity of −31 dBm. The RF-powered fully-passive WuRX paves the way for autonomous batteryless sensor nodes.**

***Index Terms*—RF energy harvesting, fully-passive wake-up receiver (WuRX), sensitivity, small loop antenna, ultra-low-power.**

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART PASSIVE AND ULTRA-LOW-POWER WURXS

	This work	IoT-J'19 [6]	NXP UCODE 9 [5]	TCASII'18 [13]	JSSC'21 [12]	TCASII'19 [10]
Node	**130 nm**	130 nm	40 nm	130 nm	180 nm	130 nm
Freq. [MHz]	**830**	915	868	900	433	2400
Architecture	**Passive, RF-DC conv., ED-first RX, small loop ant.**	Passive, RF-DC conv., ED-first RX	Passive, RF-DC conv., ED-first RX EPC mem.	Semi-passive, ED-first RX, match. netw.	Semi-passive, ED-first RX, small loop ant.	Semi-passive, ED-first RX, match. netw.
Internal reg.	**VREF, IREF, LDO, POR**	VREF	VREF, IREF LDO, POR	VREF, IREF	N/A	N/A
Modulation	**OOK**	OOK	OOK	OOK	OOK	OOK
Bitrate [kbps]	**26**	1	20	31	0.2	2.5
Code length	**12**	N/A	N/A	N/A	16	N/A
Passive gain [dB]	**26**	23	-	25	16	6.4
Power [nW]	**0**	0	0	500	3	100
Latency [ms]	**2**	N/A	1.4	N/A	80	N/A
Sensitivity [dBm]	**-30.7**	-26	-24	-35	-65	-48.5
SIR [dB]	**-9**	0	-	-	-47	-

VREF = voltage ref.; IREF = current ref.; SIR measured at 3 MHz offset

I. INTRODUCTION

INDUSTRY surveys show that batteries are the bottleneck for scaling IoT devices due to their limited lifetime and replacement costs [1], [2]. For IoT devices mostly in idle mode, the battery life can be extended by including a wake-up receiver (WuRX) which keeps the node in sleep mode unless woken up [3]. The recent ultra-low-power WuRXs with nW–μW power are limited by their power consumption and the dependence on battery [4]. This power consumption can be reduced using a fully passive WuRX powered by an RF energy harvester. A passive WuRX listens to the communication channel once powered up by the harvested input RF energy, waking up the IoT node on command. The additional benefit of a passive WuRX is the possibility of directing excess harvested energy to a storage unit and, thus, enabling autonomous batteryless IoT nodes [1], [5].

The architecture of the proposed WuRX is comparable to recent passive [6] and ultra-low-power WuRXs [7], [8], [9], [10], [11], [12], [13], [14], which operate at various sub-10 GHz frequencies. Due to their nW power budget, they utilize envelope detector (ED)-first RX architectures [4]. The RF down-conversion is done passively, allowing the WuRXs to operate at nW power levels, though often at the cost of sensitivity. They only support on-off keying (OOK) modulated input signals. The ED-first architecture can be fully passive or ultra-low-power by relying on external bias circuits and input RF signals. Unlike the ultra-low-power WuRXs in [4], [7], [8], [9], [10], [11], [12], [13], [14], the proposed WuRX is fully passive, and it relies on RF energy harvesting. To the best of our knowledge, this is the lowest sensitivity fully passive RF WuRX supporting a 12-bit wake-up pattern at 26 kbps as detailed in Tab. I. In addition, the high input impedance of an ED-first receiver results in the requirement of a high quality (Q) factor matching network and a 50 Ω antenna or a conjugate-matched antenna. Both approaches provide a voltage boost at the input of the ED and improve the WuRX sensitivity by up to 20 dB [4]. The approach with a matching network is a sub-optimal solution because of its high insertion loss and the use of area-consuming passive elements [15]. To avoid this, the proposed WuRX includes a conjugate-matched small loop antenna which provides a 26 dB voltage gain at the input.

II. WURX ARCHITECTURE

Fig. 1 shows the block diagram of the proposed passive WuRX, including a matched small loop antenna. The CMOS RF frontend of the WuRX consists of an RF-DC converter, which harvests the incoming RF energy to DC energy. The power management sub-system consists of a voltage-current

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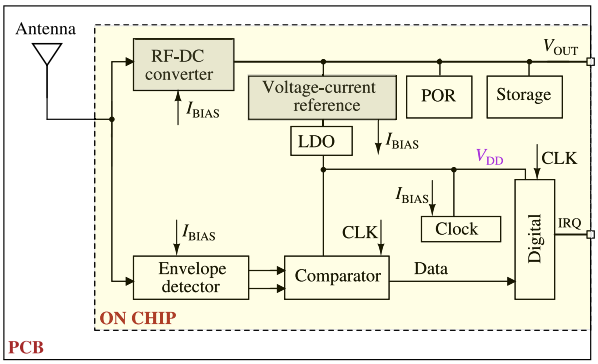

Fig. 1. System overview of the fully passive WuRX including a small loop antenna: The WuRX includes a pre-designed RF-DC converter [16] and voltage-current reference [17].

reference (0.47 V, 2 nA), a power-on reset (POR), and a low-dropout regulator (LDO). The internal LDO output 0.55 V supplies the relaxation oscillator, comparator, and digital correlator supply voltage to enable a low-voltage low-power operation. The input signal of the WuRX after successful startup is processed by an ED-first receiver which includes an ED, comparator, and a digital processor. The digital correlator continuously compares the input signal with a set 12-bit wake-up pattern with 2x oversampling factor at 26 kbps bitrate.

In this brief, the WuRX is enabled by several innovations: (I) The WuRX includes an RF-DC converter and an ED whose rectifying CMOS diodes are threshold-compensated using a dedicated central current reference I_{BIAS} (see Fig. 2a,b,e). The threshold compensation of the rectifying diodes helps reduce the effective turn-on voltage and rectify low-amplitude input signals and, thus, achieve high WuRX sensitivity, i.e., the minimum input power to operate the passive WuRX. The RF-DC converter fully supplies the sub-blocks of the WuRX. (II) All of the MOS transistors used in the WuRX are designed to work in the sub-threshold region. The WuRX sub-blocks relaxation oscillator, the comparator, and the digital processor are designed in a low internal 0.55 V supply voltage to ensure an ultra-low power consumption. (III) The WuRX includes a novel shared-resistive relaxation oscillator which reuses an internal sub-50 mV reference voltage V_{SUB} generated in the current-reference circuit (see Fig. 2c, f).

A. Block-Level Design

1) RF-DC Converter: The RF-DC converter shown in Fig. 2a is an enhanced five-stage Dickson charge pump whose rectifying CMOS diodes are threshold-compensated [16]. The rectifying CMOS diodes shown in Fig. 2b comprise a primary and a complementary transistor. The threshold compensation is done using a 2 nA bias current I_{BIAS} generated from the current reference block (see Fig. 1). The bias current I_{BIAS} taken from the current reference of the WuRX helps to create an optimum voltage drop across the complementary diode. The voltage drop biases the gate node of the primary rectification diode at a precharged voltage level, resulting in a slightly forward-biased rectifying diode. The RF-DC converter is optimized to achieve a sub-μW startup and a good power conversion efficiency to supply the energy for the various sub-systems of the passive WuRX (peak efficiency of 53% at −18 dBm input power for 1 MΩ load).

2) Voltage-Current Reference and POR: The strict performance requirements of a WuRX demand a high-accuracy voltage-current reference with a low supply voltage startup [3], [4]. The voltage-current reference shown in Fig. 2c is a reuse of the work in [17] (0.47 V V_{REF}, 2 nA I_{BIAS}, 40 mV V_{SUB}), with a minimum supply voltage of 0.9 V. The voltage-current reference is temperature compensated across a range from −40 °C to 120 °C. The POR circuit shown in Fig. 2c generates the reset signal for the WuRX. It ensures that the WuRX is initialized only when the harvested voltage crosses a predefined threshold value of 0.9 V for the voltage-current reference to startup and the digital logic gates to function.

3) LDO: The LDO shown in Fig. 2d consists of three main blocks: an error amplifier (EA), a pass transistor driving an output load, and a feedback network. The resistive feedback network has been designed using PMOS diode transistors to avoid large MΩ resistors required for 5 nA quiescent current. The voltage reference input 0.46 V V_{REF} is taken from the voltage-current reference. The LDO stability is achieved using cascaded compensation, making the EA output the dominant pole [18] and a minimum phase margin of 50°, thus relaxing the LDO output's load requirements. As the ultra-low-power LDO is too slow to react to large current spikes from the switching at the load oscillator and digital correlator, a minimum on-chip 20 pF capacitance is required to keep the output within a specific error window of 20 mVp-p. The power supply rejection ratio PSRR, as seen in simulations, is 60 dB @ 1 Hz.

4) Envelope Detector: The pseudo-differential ED in [8], [11] uses a Dickson topology-based ED where the MOS transistors are used in diode-configuration for rectification. The minimum input voltage required to turn on these MOS transistors typically depends on their threshold voltage. To overcome this, [12] uses a 30-gain stage Dickson charge pump to increase the overall voltage gain at the cost of a bulk circuit with parasitic input capacitance to the ground. This increases the circuit's Q factor, which makes it harder to design a matched antenna for the WuRX. The proposed ED in this brief (see Fig. 2e) avoids a bulky analog frontend using two single-stage Dickson charge pumps with modified CMOS diodes. The modified CMOS diodes (see Fig. 2b) are threshold-compensated using the 2 nA I_{BIAS}. The low turn-on voltage increases the WuRX sensitivity to low-amplitude signals. The I_{BIAS} is further used to tune the ED slew rate depending on the input signal bitrate.

5) Clock: The on-chip clock is a dual-phase shared-resistive 7 nW 52 kHz relaxation oscillator (see Fig. 2f). The design is an improved version of [19], with a reduced 0.55 V supply voltage and first-order temperature compensation of output frequency. It reuses an internal sub-50 mV reference voltage from the current reference circuit, thus, helping to avoid the usage of large MΩ resistors needed to achieve a low power operation. The startup circuit pulls the node V_{O2} to V_{SS} in case of fast supply transients to avoid a false operating condition of the oscillator wherein the intermediate nodes V_{O1} and V_{O2} both get pulled to V_{DD}.

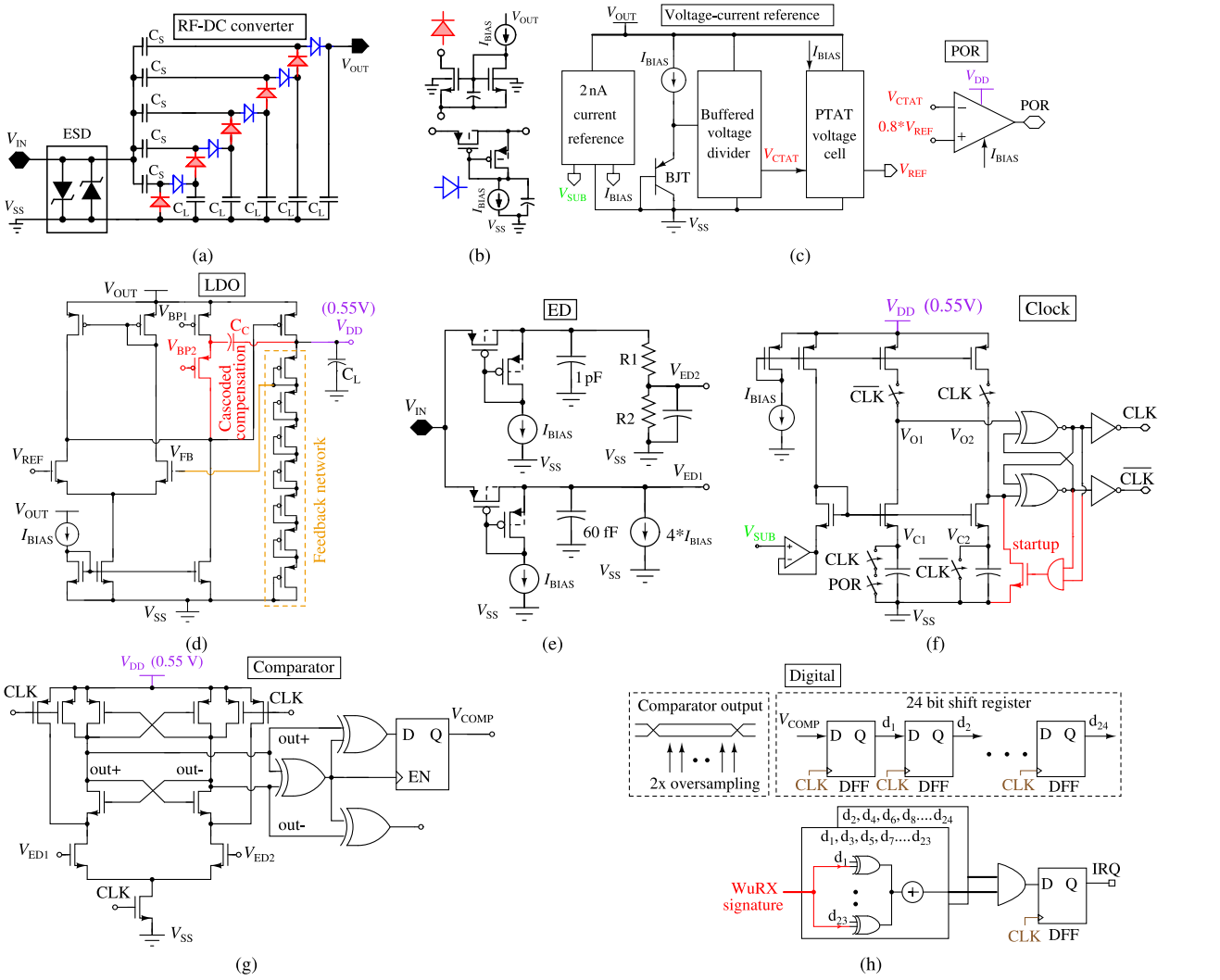

Fig. 2. (a) System overview of the RF-DC converter using threshold-compensated CMOS rectifying diodes [16], (b) threshold-compensated NMOS and PMOS diode construction, (c) block diagram of the proposed voltage-current reference [17] and POR circuit, (d) simplified schematic of the LDO to scale $V_{REF} = 0.47$ V to reference voltage $V_{DD} = 0.55$ V, (e) schematic of the ED which uses modified threshold-compensated PMOS rectifying diodes, (f) schematic of the dual-phase shared-resistive relaxation oscillator, (g) schematic of the modified strong-arm latched comparator, and (h) the 12-bit 2x oversampled digital correlator.

6) Comparator: The clocked comparator shown in Fig. 2g is an improved strong-arm latched comparator [20] with zero static power and rail-to-rail output. The sub-threshold operation of the transistors due to the low supply voltage level results in a limited slew rate of the output nodes. A slow slew rate causes potential issues by triggering a false switching of the digital gates, especially when the intermediate nodes out- and out+ are at $V_{DD}/2$. The additional XOR gate between the nodes out- and out+ improves the driving capability and ensures an output decision only when the nodes are at different logic levels. It is used as enable signal for the output latch of the comparator.

7) Digital Correlator: The latched output of the comparator is fed to the 12-bit shift-register-based correlator, which is also supplied by the intermediate 0.55 V V_{DD} supply (see Fig. 2h). A 2x oversampling helps to avoid phase synchronization issues between the incoming signal and the clock. The wake-up pattern is fixed programmed as 101010101010 using tie-zero and tie-one cells in the design, and the IRQ signal is generated when one of the parallel signal detection paths ($d_1, d_3, \ldots .d_{23}$ or $d_2, d_4, \ldots .d_{24}$) successfully detects the wake-up pattern.

The passive WuRX is designed with a target wake-up sensitivity of less than −30 dBm. The input impedance of the WuRX, as seen in post-layout simulations, is (1.5-j230) Ω at 830 MHz at an input power of −30 dBm. Fig. 3a shows the microphotograph of the passive WuRX fabricated in an in-house 130 nm CMOS process. The active area of the WuRX is 0.2 mm^2. The passive WuRX is part of a 16 mm^2 test chip mounted directly on a printed circuit board (PCB). The test chip includes an external power supply for the calibration circuit and the output buffers. The capacitive nature of the input impedance of the WuRX demands the design of a matched antenna whose reactance is inductive. A small loop antenna with an inductive reactance [21] is co-designed with the WuRX to achieve resonance at roughly 830 MHz. The matched small loop antenna (size: 22 mm x11 mm, width: 1.5 mm) is designed using Ansys HFSS and has a simulated

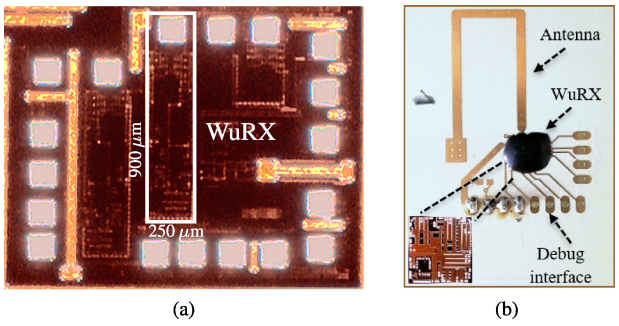

Fig. 3. (a) Die microphotograph of the WuRX and (b) 16 mm^2 Rogers PCB, which includes the passive WuRX and the matched small loop antenna.

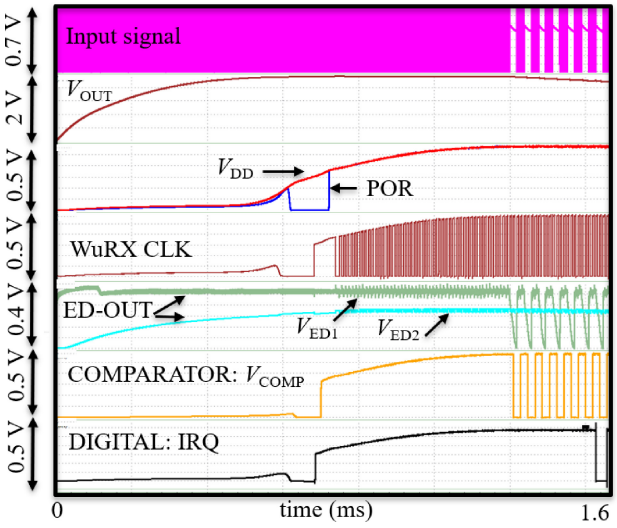

Fig. 4. Simulation results of the passive WuRX: OOK modulated input RF signal, harvested output voltage V_{OUT}, internal 0.55 V supply voltage V_{DD}, POR to signal the startup of the WuRX, clock output CLK, ED output signals V_{ED1} and V_{ED2}, the comparator output signal V_{COMP}, and wake-up output signal IRQ (active low). Input bitrate of 26 kbps at 830 MHz; wake-up code: 101010101010.

impedance of $(1.5+\mathrm{j}\,230)\,\Omega$ at 830 MHz, and a peak gain of 1 dBi. It provides a voltage boost of 26 dB at the WuRX input. Fig. 3b shows the passive WuRX, including the small loop antenna, on a 0.3 mm Rogers 4350B PCB. The debug interface shown in Fig. 3b helps to calibrate the individual WuRX sub-blocks like voltage-current reference and oscillator frequency and probe the WuRX test signals.

III. Simulation and Measurement Results

Fig. 4 shows the working principle of the WuRX, as seen in simulations. Once the harvested output voltage V_{OUT} crosses the startup threshold, the internal supply voltage V_{DD} is generated, and the POR is triggered. The POR signals the start of the oscillator and the signal processing sub-system. The ED designed using threshold-compensated CMOS diodes demodulates the incoming OOK signal (V_{ED1}) and also generates the average detector output (V_{ED2}), and feeds the signals to the comparator. The digital processor oversamples the output signal V_{COMP} of the comparator and compares it with the set wake-up pattern. The wake-up signal IRQ is pulled to the ground (active low) upon correct pattern detection.

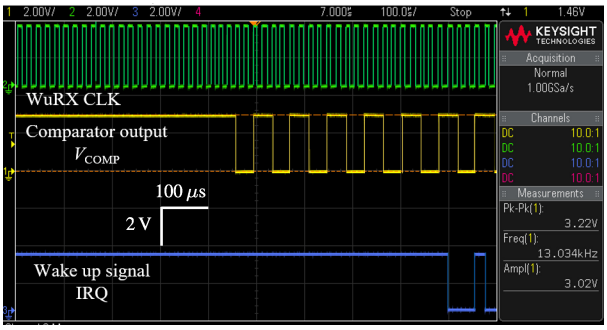

Fig. 5. Measurement results of the passive WuRX to show the working functionality (screenshot): Internal relaxation oscillator clock, comparator output signal, and the wake-up signal IRQ at the output of the digital correlator. Input bitrate of 26 kbps at 830 MHz, wake-up code: 101010101010.

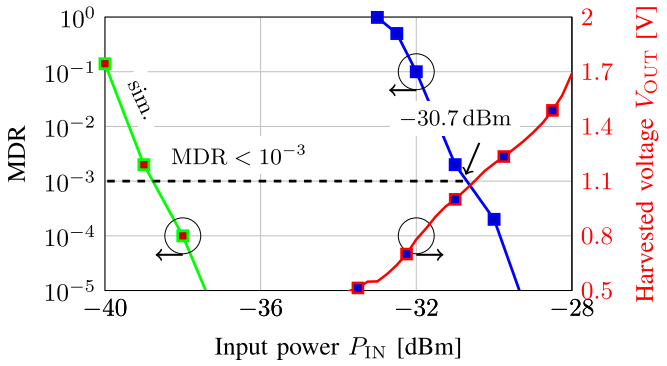

Fig. 6. Measurement and simulation results of the passive WuRX: MDR at an input bitrate of 26 kbps (blue: measurement, green: simulation) and the harvested voltage V_{OUT} versus input power P_{IN} (red: measurement). The RF harvester has a 1 V sensitivity of −31 dBm (f = 830 MHz).

The WuRX measurement setup consists of a signal generator to generate the input signal, an oscilloscope to probe the WuRX output signals, and a digital multimeter to measure the harvested signal V_{OUT}. The input power is determined using a reference hyper-log 7040 antenna and a spectrum analyzer. The transient response of the WuRX to the wake-up signal is shown in Fig. 5. It shows the WuRX clock, powered by the harvested energy, running at 52 kHz. The comparator successfully detects the input OOK-modulated signal. The exemplary wake-up pattern of 101010101010 to prove the concept is detected by the digital processor. As a result, the output signal IRQ goes low. The latency of the WuRX is 600 μs, determined by the input bitrate and the 12-bit wake-up sequence.

The passive WuRX achieves a wake-up sensitivity of −30.7 dBm, with a missed detection rate (MDR) of 10^{-3} at a bitrate of 26 kbps (see Fig 6). The sensitivity of the WuRX with an ideal supply voltage and bias current, as seen in simulations, is −38.5 dBm. The ED sensitivity is limited by the effective input voltage after subtracting the diode voltage drops of the rectifying diodes. Fig. 6 also shows the harvested output voltage V_{OUT} versus available input power P_{IN}. The WuRX achieves 1 V at the output V_{OUT} at −31 dBm P_{IN}. The results in Fig. 6 indicate that the WuRX reaches a reliable operational state at $P_{IN} > -31$ dBm. The WuRX sensitivity is improved due to the threshold-compensated CMOS diodes, which help detect low-amplitude input signals.

The OOK modulation scheme of the ED-first RX results in all in-band signals amplified [4]. This results, in general,

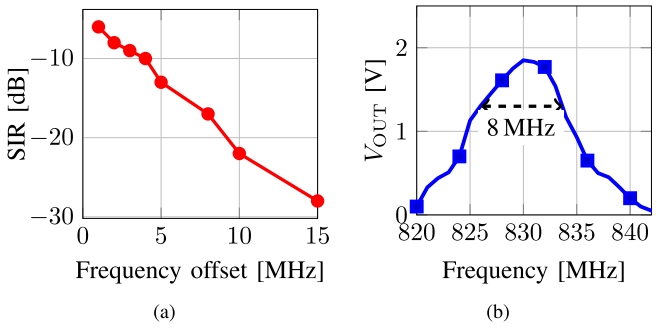

Fig. 7. Measurement results of the WuRX: (a) SIR ($f = 830$ MHz) and (b) the frequency response of the WuRX ($P_{IN} = -28$ dBm).

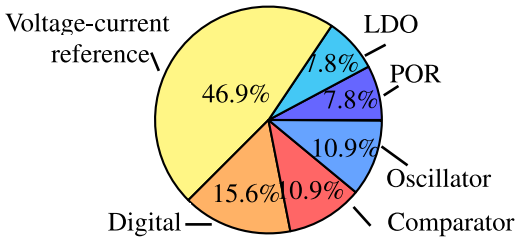

Fig. 8. Simulated power consumption of the individual blocks supplied by the harvested output energy: The total power consumption at 27°C is 64 nW.

in a limited signal-to-interference ratio (SIR) and high sensitivity to interferer signals in the bandwidth of the small loop antenna. Measurements reveal a SIR of −9 dB at 1 MHz offset (see Fig. 7a). The SIR is boosted due to the narrow 8 MHz bandwidth of the WuRX (see Fig. 7b). The narrow bandwidth arises from the high Q factor of the small loop antenna.

The WuRX sub-blocks supplied by the RF-DC converter consume a total power of 64 nW at room temperature, as shown by simulation in Fig. 8. The voltage-current reference dominates with a power consumption of 30 nW.

Compared to the reported WuRXs in Tab. I, this is the first fully passive RF-powered WuRX, including a small loop antenna. The internal regulation, including a voltage-current reference, a POR, and an LDO, is fully integrated into the WuRX. The superior latency of the WuRX compared to the related works in Tab. I arises from the faster internal clock, and it is highly beneficial for emerging industrial applications [4]. The wake-up sensitivity of the presented fully passive WuRX is much lower than the ultra-low-power WuRXs in Tab. I. It is because of the minimum input power required by the RF-DC converter to start the WuRX. The presented WuRX and the passive WuRXs in [5], [6] are limited by the start-up sensitivity of the inbuilt RF-DC converter.

IV. Conclusion

This brief presents a novel fully passive RF WuRX, including a small loop antenna with a sensitivity of −30.7 dBm. The passive WuRX supports a 12-bit wake-up pattern at a 26 kbps bitrate. Integration of the WuRX is achieved using an ED-first RX, a voltage reference, a current reference, a power-on reset, an LDO, and a comparator. Compared to the related works, the fully-integrated passive WuRX relies on RF energy harvesting, and it paves the way for autonomous batteryless sensor nodes.

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