Behavioral Model of UHF RFID Tag for System and Application Level Simulation

Vojtech Derbek, Christian Steger, Suad Kajtazovic
Institute for Technical Informatics
Graz University of Technology, Austria
{derbek, steger, kajtazovic}@iti.tugraz.at

Josef Preishuber-Pfluegl, Markus Pistauer
CISC Semiconductor Design + Consulting GmbH
Klagenfurt, Austria
{j.preishuber-pfluegl, m.pistauer}@cisc.at

ABSTRACT

In this paper, we present a model of an UHF RFID tag for system and application level simulation. The prime focus is on the radio frequency link. The model describes carrier frequency dependent behavior based on the envelope signal description with the value of the carrier frequency being time invariant parameter. The background idea is to model the ASIC load current as a time variant function of the load voltage and to keep ASIC parallel reactance time invariant.

1. RELATED WORK

Limitations of passive RFID (Radio Frequency IDentification) transponders operating in 125 kHz or 13.56 MHz frequency bands are recently avoided by the introduction of 900 MHz based transponders where applicable. UHF (Ultra High Frequency) tags achieve higher communication ranges, higher data rates, and smaller antenna sizes. Better performance of ultra high frequency RFID systems implies more complex design on the system integration level. Currently product development of UHF RFID is done by simulations based on product models of different complexity, which is then used to select certain components or by producing semiconductors based on the simulated models.

System evaluation on low abstraction levels in respect to the period of the carrier frequency and the signal itself involves computations with the simulation step time in the order of 10^{-8} s. UHF RFID systems have typically a data rate from 40 to 160 kHz in the forward link (reader-to-tag) and depending on given standard and RF regulatory environment up to 640 kHz in the return link (tag-to reader). Due to the fact that the ratio between data and carrier frequencies is in the order of thousands to tens of thousands, evaluating a communication protocol requires simulation time step several 10k times lower than the period of one bit in the data stream. Such a high accuracy is however not required neither for the simulation of the protocol itself nor by the tag circuitry, except the front end radio frequency link. Replacement of the carrier frequency modeling by the envelope signal based modeling methodology is the basic building strategy for achieving shorter simulation times with highly reliable description of critical signals across multiple abstraction levels. Figure 1 shows the framework of the developed UHF RFID model for system and application level simulation. This paper focuses on the tag front-end module.

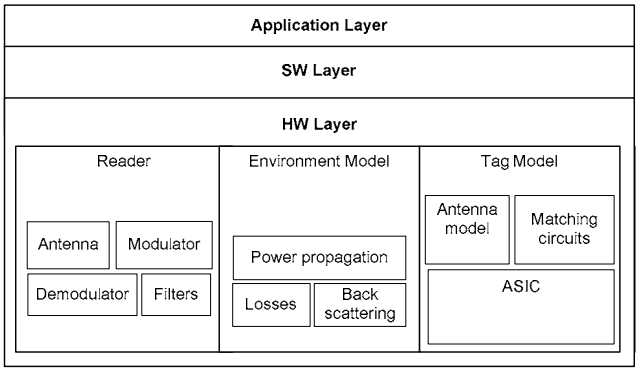

Figure 1: Structure of UHF RFID system for the system, communication protocol and hardware evaluation

Several research works [1],[2],[3] consider properties of an UHF system and present models for the evaluation of individual components. A study [4] presented a framework for an RFID behavioral model with the stress on the antenna parts of the transmitter and the receiver using VHDL-AMS language.

In this paper we present a Matlab/Simulink based model extending above listed properties further to the evaluation of both reader and tag analog and digital modules. The model is developed in respect to the behavior driven by the carrier frequency wave, and in respect to the time span necessary for the evaluation of the communication protocol. The tag ASIC and radio frequency link is of particular interest.

2. MODEL OF AN UHF RFID TAG

2.1 Behavioral model of the RF link

Radio frequency link is the part of the UHF RFID system in which the carrier frequency signal takes effect directly. Starting with the reader modulator, the carrier signal is present in entire environmental model and in the tag front-end.

Power transmitted by the interrogator is propagated in the form of an electromagnetic wave with a frequency f_c of the

carrier signal. Data is modulated on the carrier wave with a certain waveform in respect to the signal bandwidth requirements, data encoding, and other.

In a typical application setup, the reader antenna is placed in a plastic cover preventing the tag to get closer to the antenna than approximately 5 cm. In the UHF frequency range (860 – 960 MHz) is this distance already in the far field for electrically small antennas. The corresponding power P_{tag} available to the tag can be computed based on the reader transmit power according to the Friis formula.

$$P_{tag} = P_{reader} G_{reader} G_{tag} \left(\frac{\lambda_c}{4\pi d} \right)^2, \quad (1)$$

where P_{reader} is the power transmitted by the reader, G_{reader} and G_{tag} is the reader and tag antenna gain respectively, λ_c is the wavelength of the carrier signal, and d is the distance between the reader and the tag.

Having an UHF RFID system with the reader transmitting P_{reader} = 1 W EIRP with the antenna gain G_{reader} = 6 dB on the carrier frequency of 900 MHz, and a tag antenna gain G_{tag} = 2 dB, the power P_{tag} available to the tag at the distance of 0.05 m will be 1.77 W. This is the maximum power assumed in the model for the evaluation of the radio frequency coupling circuit.

The model of the tag comprises a model of the tag antenna (2) and a model of the tag ASIC (3) as depicted in Figure 2. A voltage U_L appears across the signal pads of the tag ASIC. The antenna is modeled as a serial circuit of an AC voltage source U_0, resistance R_a, and inductance L_a. The tag ASIC is modeled as a general impedance Z_c that is defined either as a serial wiring of a resistance R_s and a capacitance C_s (Figure 2), or as a parallel wiring of a resistance R_p and a capacitance C_p. Typical ASIC input impedance value is in the order of 10^1 Ω for the real part and 10^2 Ω for the imaginary part.

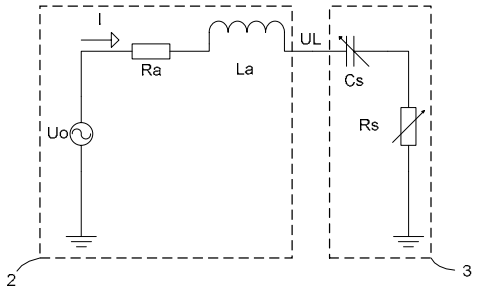

Figure 2: Equivalent circuit of an RF-transponder in a serial layout

In order to bring a maximum of the tag RF available power to the DC part, the antenna has to be matched to the tag ASIC. This yields following identity:

$$Z_a = Z_c^*, \quad (2)$$

where Z^*_c is the complex conjugate to the antenna impedance.

Impedance of the tag is not constant even if the tag is not in the transmitting mode, changing its matching coefficient. The tag resistance changes according to the actual load current, which is most of all dependent on the state of the buffer capacitor and available power level.

An UHF RFID tag comprises of an antenna including the matching circuitry, and tag ASIC as depicted in Figure 1. The analog model of the tag ASIC is build up of three basic blocks - rectifier, parallel voltage controller and data modulator/demodulator. The digital part of the model includes the digital logic and the memory. Based on the input voltage U_L signal and the structure of individual blocks the signal of the load current I_L is computed.

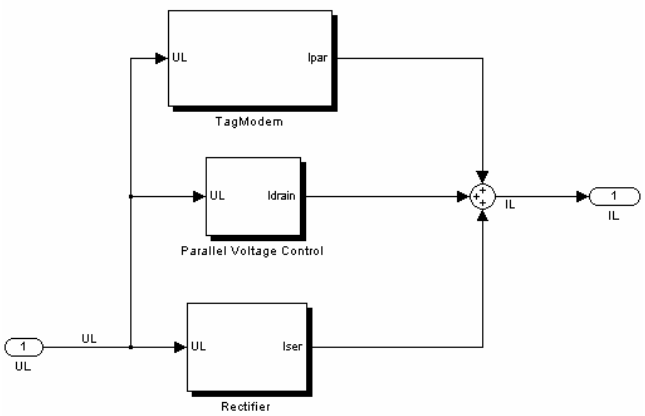

Figure 3: Tag ASIC Simulink block model

Figure 3 shows the basic block structure of such a model. Individual blocks include further components. The input voltage is represented as a rectified envelope signal* and the dynamic response of these components is significantly slower than the response of the tag RF circuitry.

The tag ASIC block is therefore modeled as a variable resistance R_p being a function of load voltage U_L.

$$R_p = R_p(U_L) \quad (3)$$

The equivalent circuit of the RF transponder can be then expressed as a serial circuitry with one variable component R_p according to figure 4. The R_p block is modeled in the form of a structure shown in figure 3.

* The rectifier block accepts an envelope of U_L voltage at its input and models the rectifier efficiency instead of doing real rectification.

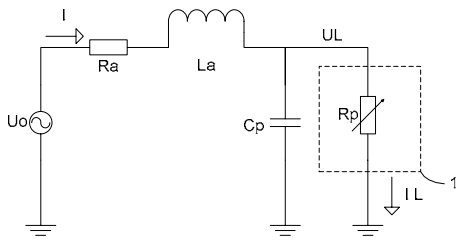

Figure 4: Equivalent circuit of an RF-transponder in a parallel layout

Serial resistance and reactance are the functions of X_p and R_p.

$$R_s = \frac{R_p X_p^2}{R_p^2 + X_p^2} \tag{4}$$

$$X_s = \frac{R_p^2 X_p}{R_p^2 + X_p^2} \tag{5}$$

2.2 Tag RF circuitry model

As discussed, simulating the tag RF circuitry requires the presence of the carrier signal. For the purposes of the system evaluation we developed model of the circuitry based on a pre-computed lookup table in the form

$$U_L = U_L(P_{tag}, I_L) \tag{6}$$

where U_L, P_{tag}, and I_L are represented by the envelopes of the real signals. The U_L voltage is of particular interest as this signal is the input to the ASIC blocks.

The power received by the tag and available for the DC voltage generation is given by

$$P_{tag} = \frac{1}{2}\mathrm{Re}(u_0 \cdot i) \tag{7}$$

and for the magnitude can be therefore derived

$$|P_{tag}| = \frac{1}{8} \cdot \frac{U_0^2}{R_a} \cdot (1 - \gamma^2) \tag{8}$$

where

$$\gamma = \frac{Z_c - Z_a^*}{Z_c + Z_a}. \tag{9}$$

The magnitude of U_0 is therefore given by

$$|U_0| = \sqrt{\frac{8 P_{tag} R_s}{(1 - \gamma^2)}} \tag{10}$$

Typical value of the load current I_L ranges from 10^{-6} to 10^{-5} for low input power values*. In extreme case of the 2 W input power the current drained by the parallel voltage regulator might be up to 100 mA. As the tag ASIC is modeled as a parallel wiring of a time invariant capacitance and time variant resistance, the load current is given by

$$I_L = \frac{U_L}{R_P}. \tag{11}$$

Finally the magnitude of U_L is

$$|U_L| = |U_o| \sqrt{\frac{R_s^2 + X_s^2}{(R_a + R_s)^2 + (X_a + X_s)^2}}. \tag{12}$$

2.3 RF link model evaluation

2.3.1 Functionality validation

We used numerical solution of equations (3), (4), (5), (9), (10), (11), and (12) to evaluate the function of two variables according to (6) for possible values of the tag input power and load current. Figure 5 presents a plot of U_L over I_L and P for a tag with ASIC input impedance of 30 – j250 Ω. Even if modeled U_L maximum is above 100 volts for the input power of 2 W and low I_L currents, this value is never achieved due to the on-chip voltage regulator that starts draining the current already at U_L = 3 V causing a mismatch to prevent tag damage by high voltage. This principle is reflected in the model by the Parallel Voltage Control block.

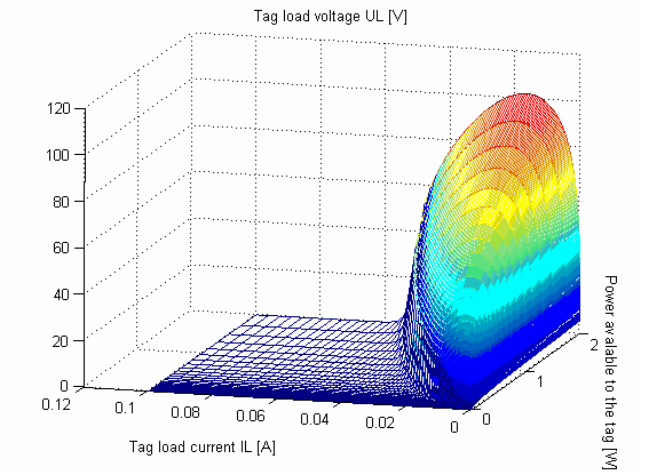

Figure 5: UL for Zasic = 30 – j250 Ohm

A similar behavior should be expected when the tag transmits data on the return link. When changing the reflection coefficient the tag ASIC changes actually its

* Power values at which the parallel voltage regulation does not take effect.

impedance by switching the modulating transistor on and off. This results in increased circuit currents and, as a side effect, decreased voltage on the ASIC signal pads. This behavior can be clearly observed in figure 6. The figure shows typical values of tag signals (tag data [top scope], envelope of the voltage U_L on tag signal pads, and DC voltage [bottom scope]). The ASIC serial input impedance was 30 - j250 Ω at 870 MHz carrier frequency. The input RF power at the tag was 450µW. and further power losses occurred due to non-optimal matching of the tag IC and the antenna.

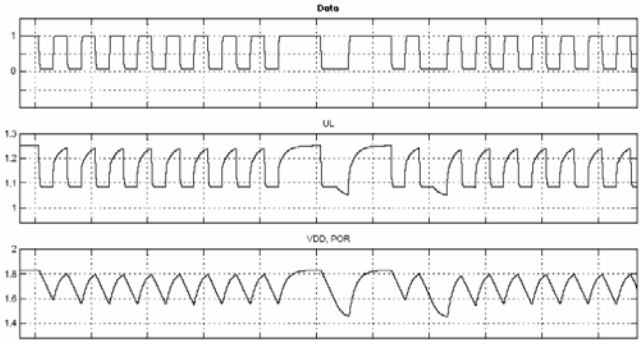

Figure 6: Simulation output: Signals on the tag

The simulation results were compared to the measurements on an RFID tag with EM4022 IC [6]. Aside of the antenna pads, the ASIC includes test pads for measurements and test signals inputs. Figure 7 presents the measured DC voltage supply for the digital logic under the same conditions as used for the simulation. The tag shows significant DC voltage drops during the modulation phase. This has a significant impact on the tag operation ability in far distances from the reader where power on reset might occur.

Figure 7: Measurement output: Lower signal: Tag serial data*, Upper signal: Tag DC voltage

* Rectangular data signal is distorted by measuring on an IC test pin designed for different primary use. This did not affect the tag functionally and on-tag signals.

2.3.2 Use in application level modeling

The presented UHF tag RF front-end model has been complemented with an implementation of communication protocols and included in a model of an RFID reader gate with four antennas. Each antenna is specified by its position, rotation, and radiation pattern according to given specification. The model is used for simulating of various effect like power fading caused by dense reader environments, or impacts of antenna multiplexing generating on/off power ramps and causing faulty data on the input of the tag digital part. Simulation of tags moving through reader gate show the actual level of DC voltage, input signal, demodulated data and generated response.

3. CONCLUSION

We presented a model of an UHF RFID tag for the evaluation of signals on tag modules in respect to different ASIC implementations, communication parameters, and system properties. The model has been validated by measurements on a real tag. The use of behavioral model brought the possibility to do application and system-level model-based evaluation of UHF RFID in respect to given component specifications.

The current research is focusing on real-time evaluation and model-based automated prototyping by bringing the model on target RT architectures (DSP/FPGA).

4. REFERENCES

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