Originalarbeit

Elektrotech. Inftech. (2024) 141:66–75
https://doi.org/10.1007/s00502-023-01200-x

e+i elektrotechnik und informationstechnik

Influence of the IC power supply and decoupling capacitor arrangement on the electromagnetic emission

B. Deutschmann · N. Juch

Received: 23 October 2023 / Accepted: 6 December 2023 / Published online: 10 January 2024

Abstract With the advancing development of integrated circuits (ICs), more and more complex functions and higher performance levels can nowadays directly be integrated into a single IC package. In this context, the issue of electromagnetic compatibility (EMC) is becoming more critical, as the higher the integration density, the higher the electromagnetic emissions tend to be. In this paper, an EMC test IC is used to investigate the influence of different power supply pinouts (arrangement of VDD and GND pins in center and corner configuration) on the electromagnetic emission of the IC. This is done on the basis of the surface-scanning technique described in the IEC 61967-3 standard for characterizing the magnetic near field at the surface of the IC package, and on the basis of the 150 Ohm measurement method described in IEC 61967-4 for determining the conducted interference emissions at the power supply pinout of the IC. Both measurement methods show a significant difference in electromagnetic emissions due to the dependence on the arrangement of the power supply pinouts. These results highlight the importance of careful power supply design in the development of electromagnetically compatible ICs.

Keywords Electromagnetic emission · Integrated circuit packaging · Decoupling capacitor · Advanced package technology · Pinout · Surface scan · H-field measurement · IEC 61967 · 150 ohm method

B. Deutschmann (✉) · N. Juch
Institute of Electronics (IFE), Graz University of Technology, Inffeldgasse 12/I, 8010 Graz, Austria
bernd.deutschmann@tugraz.at

Einfluss der Anordnung von IC-Stromversorgung mit Stützkondensatoren auf die elektromagnetische Emission

Zusammenfassung Mit der fortschreitenden Entwicklung integrierter Schaltkreise (ICs) können heutzutage immer komplexere Funktionen und höhere Leistungsstufen direkt in ein einziges IC-Gehäuse integriert werden. In diesem Zusammenhang wird die Frage der elektromagnetischen Verträglichkeit (EMV) immer kritischer, denn je höher die Integrationsdichte ist, desto höher sind tendenziell auch die elektromagnetischen Emissionen. In diesem Beitrag wird ein EMV Test-IC verwendet, um den Einfluss von verschiedenen Stromversorgungs-Pinouts (Anordnung der VDD- und GND-Pins in Center- und Corner-Konfiguration) auf die elektromagnetische Emission des ICs zu untersuchen. Dies geschieht auf der Grundlage der in der Norm IEC 61967-3 beschriebenen Surface Scanning-Methode zur Charakterisierung des magnetischen Nahfeldes an der Oberfläche des IC-Gehäuses sowie auf der in der IEC 61967-4 beschriebenen 150 Ohm-Messmethode zur Bestimmung der leitungsgeführten Störemissionen am Stromversorgungsanschluss des ICs. Bei beiden Messmethoden zeigt sich ein signifikanter Unterschied in der elektromagnetischen Störemission, der auf die Abhängigkeit von der Anordnung der Pinbelegungen der Stromversorgung zurückzuführen ist. Diese Ergebnisse verdeutlichen die Wichtigkeit einer sorgfältigen Planung der Stromversorgung bei der Entwicklung von elektromagnetisch verträglichen ICs.

Schlüsselwörter Elektromagnetische Störemission · Integrierte Schaltung · Stützkondensator · Anordnung der Versorgungpins · IC-Gehäuse · Magnetisches Nahfeld · IEC 61967 · 150 Ohm-Methode · Surface Scanning-Methode

1 Introduction

The EMC of electronic devices and systems has historically been addressed at the Printed Circuit Board (PCB) and system level. Today, with the introduction of compact system-on-chip (SOC) technologies, it is increasingly necessary to address EMC issues directly at the package and IC level. As ICs continue to evolve with increasing complexity and performance, the adoption of advanced package technologies becomes essential to accommodate the growing number of functionalities and I/O pins of future IC designs. The continuous transformation has given rise to various IC package types, ranging from Dual In-line Packages (DIPs) to Small-Outline Packages (SOPs), Chip-Scale Packages (CSPs), Ball Grid Arrays (BGAs), and Multi-Chip Packages (MCPs). Packaging has become an integral aspect of IC design, typically with a focus on meeting the performance requirements of high-speed applications while minimizing the impact of parasitic effects. In this context, issues such as signal and power integrity as well as EMC play an increasing role in IC package design. By focusing on optimal arrangement of the power supply, efficient signal and power integrity management, as well as careful material selection, these new packaging technologies pave the way for the development of EMC-compliant ICs.

It seems obvious that EMC performance can be improved by a suitable choice of the IC package. The influence of the IC package on the parasitic inductances e.g. in the IC's power supplies seems obvious. These inductances strongly depend on the geometry of the power supply loops and thus on package type and especially the position of the power supply pins within the package. Packages that offer a very small loop area of the power supply tend to reduce the ground bounce amplitude and thus the electromagnetic emission of the ICs. The EMC performance of IC packages was investigated in [1]. In this paper the radiated electromagnetic emission of two different types of packages Plastic Ball Grid A-ray (PBGA) and Super Ball Grid Array (SBGA) were investigated up to 10 GHz. It was shown, that SBGA packages are substantially better regarding the EMC performance and are highly dependent on the used grounding configuration. In [2], the electromagnetic radiation from IC packages and the potential electromagnetic interference (EMI) are investigated by studying the main principles and characteristics of electromagnetic radiation caused by traces and vias in the IC packages. An attempt to suppress EMI by introducing absorbing material into the IC package is presented in [3]. Thereby the IC package was coated with two different arrangements of thin absorbing materials to reduce the radiated electromagnetic emission caused by the switching activity of the IC. A systematic and fundamental investigation and modeling of the EMI behavior based on the contributions of ground lids, vias and traces of the package is presented in [4]. Basic modeling components for the emission generation are presented to help achieve appropriate guidelines for optimal design of EMI reduction of IC packages. In [5], based on studies of smart power SOCs, interactions between on-chip parasitic capacitors and parasitic package elements, as well as the resulting propagation of electromagnetic emission were demonstrated. The various interaction mechanisms such as package-to-substrate, chip-to-package, and chip-partition-to-partition feedthroughs for representative packages and ICs were investigated and quantified in terms of their EMI impact in [6].

In [7] EMI is also seen as a critical issue for the next generation of system-on-package (SOP) integrated high-performance digital, high-frequency and analog ICs. In this paper next to topics such as die-, package-, and substrate-level EMI, electromagnetic modeling and simulation, near field coupling and its related radiated emission of the IC is discussed by emphasizing signal-return path loops and power/ground line currents as EMI sources. Additionally near electric and magnetic field measurements, based on surface scanning techniques for design validation are explained. In [8], it is shown that the surface sensing method can be used for EMI root cause investigations, since it is possible to locate the sources of electromagnetic emissions based on the field distribution of electric and magnetic fields on the surface of an IC. However, measuring near fields on the surface of microchips and IC packages requires special near field probes with high resolution. The design of a fully integrated active magnetic probe is presented for example in [9].

This paper is structured as follows. Section 2 introduces the generation of electromagnetic emissions (EME) of ICs. The device under test (DUT) used for the investigation in this paper to examine the influence of the power supply pinning arrangement on the IC's conducted electromagnetic emission is described in Sect. 3. Section 4 briefly explains the used test setups for measuring the conducted as well as the near field emission of the IC. In this way, we would like to highlight how the different power supply pinning configurations influence the generated emissions, which are discussed in Sect. 5.

2 Electromagnetic emission of ICs

A large part of the electromagnetic emission (EME) of an IC is caused by the switching activities within the IC itself [10]. Especially the square-wave clock signals and the digital signals of the output drivers play a decisive role. In theory, the harmonics of these signals decrease with frequency. However, it also happens that an increase in EME can occur locally at certain frequency points. These local increases are usually caused by resonances occurring due to interactions of the IC, the IC package and the on- and off-chip decoupling capacitors.

The EME emitted by the IC depends strongly on the package, especially on the arrangement as well as the associated length of the various I/O and supply traces. This dependency can mostly be explained in three ways. The supply pins (VDD and GND) together with the pins/balls, the lead frame traces and the bond wires form conductor loops through which mostly large dynamic current peaks flow. These currents are generated by the IC's internal switching activity and usually show very high di/dt values. If such a dynamic current flows through the conductor loop formed by the power supply arrangement of the IC, magnetic fields may be emitted from these supply loops. Such magnetic fields can be visualized on the surface of the IC package and in the immediate vicinity using near magnetic field sensing techniques e.g. by using a surface scanning system. If these magnetic fields are too large, they can easily couple into conductor loops of adjacent electronic components and cause a potential EMC problem. This issue becomes more and more relevant especially at high integration densities. The larger the loop area, the better the transmitting antenna it forms. It is therefore important to arrange the IC's power supply in a way such that the supply loop area is as small as possible.

Additionally, the high di/dt causes voltage drops at the parasitic inductances of these supply loops. These voltage drops result in a potential difference of the IC's internal supply voltages compared to the supplies on the PCB. This potential difference, often referred to as "GND bounce" or "VDD bounce", occurs with the IC's operating frequency and is one reason for the IC's common mode emission [11]. Furthermore, the parasitic inductances of the loops in the IC's power supply can together with the internal or external decoupling capacitors form resonant LC circuits.

Usually, the decoupling capacitors in conjunction with these parasitic inductances form a series resonant circuit, which has a very low impedance at its series resonance frequency. This helps to allow dynamic switching currents to be shorted directly across the capacitor adjacent to the IC's power supply pins. Typically, this results in significantly smaller electromagnetic emissions around this series resonant frequency. However, it is also possible for the decoupling capacitor to combine with inductors to form a parallel resonant circuit that has a high impedance resonance. This often leads to a large voltage drop across the impedance, causing increased EME to be observed in the frequency range around the respective parallel resonant frequency.

By using techniques such as decoupling capacitors, ground planes and signal shielding, ICs with advanced package technologies can more easily meet the EMC requirements [12]. The EMC design and implementation of optimized pin configurations, especially the placement of the power supply pins (VDD and GND) within the package layout, is important. As the number of I/O pins increases, a corresponding increase in the number of power supply pins is required to minimize ground bounce interference and electromagnetic emissions. In addition, the positioning and routing of these pins within the package is critical to minimize the generation and propagation of electromagnetic emissions.

3 The device under test

The IC used to study the impact of the power supply arrangement on the electromagnetic emission was designed as an EMC test chip with multiple purposes. It allows to investigate the effects of slew rate controlled output drivers or skewing of the output signals switching timings on the EME. Further information on this test chip can be found in [13] and [14]. It was fabricated in a 0.35 µm CMOS technology with a die-size of about 1.5 × 1.5 mm. The die was mounted in a 24-pin ceramic DIP. This IC package is well suited for studying the parasitic effects of different power supply arrangements because it is very large compared to the die, and thus large loop areas are created in the power supply by long bond wires and the lead frame of the package. In principle, all results can be transferred to other package types, but in this case the values of the parasitic inductances have to be adjusted. A picture of the die and the DIP is shown in Fig. 1.

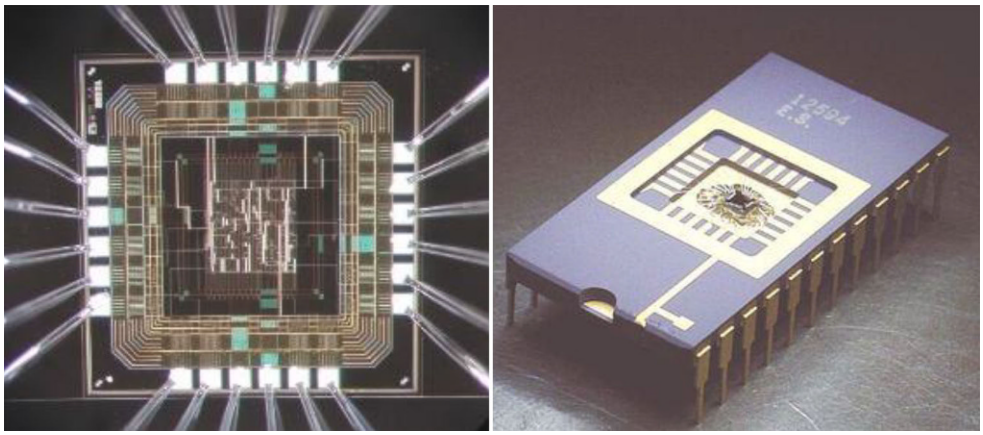


Fig. 1 Picture of the EMC test chip (die and ceramic DIP)

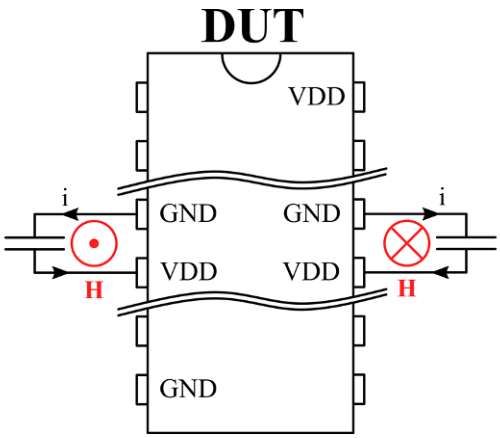


Fig. 2 Center pinning with identical VDD and GND pairs on opposite sides of the IC package

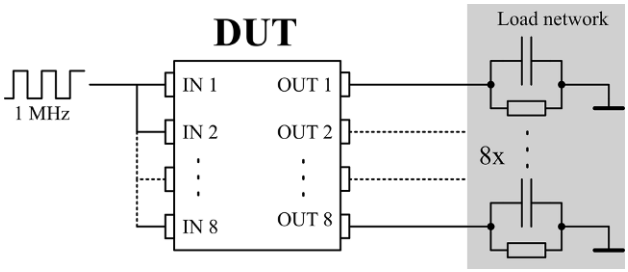


Fig. 3 Implementation of the test chip

The DUT consists of eight CMOS inputs, which are connected to eight corresponding output drivers, offering a driving strength of 8 mA. The DUT has three VDD and three GND pins, which on chip connect to a common metal structure thus providing multiple power supply connection options. One pair can be used for classic diagonal corner pinning, and the other two pairs can be used for centered pinning on each side of the IC package.

As a fundamental guideline for correctly aligning the power supply of ICs, it's imperative to minimize the loop areas formed by the power supply e.g. by using the smallest possible package, or reducing the length of the bond wires. Hence, placing the power supply pins in a manner that minimizes parasitic impedances is crucial. Typically, this involves positioning the pins so that the VDD and GND are in close proximity, leading to very small loop areas and therefore small parasitic inductances. This additionally enables the optimum placement of the decoupling capacitors between these pins on the PCB. If several identical VDD and GND pairs are used on opposite sides of the package (as shown in Fig. 2), the magnetic fields generated by the switching currents of the IC tend to cancel each other out and can therefore be significantly reduced.

For the measurements, the inputs of the IC were driven simultaneously with a 1 MHz digital signal. In order to emulate different load conditions (e.g. capacitive ones such as driving CMOS inputs, or resistive ones such as e.g. LED light indicators) the outputs were loaded with an ohmic-capacitive load (10 kOhm and 47 pF). The RC load emulates both scenarios, generates sufficient electromagnetic emission due to a large dynamic switching current to charge and discharge the capacitive load while switching at 1 MHz, and additionally provides a DC current while the output signal is in a high state via the resistive load. The implementation of the corresponding IC configuration is shown in Fig. 3.

4 Measurement of the IC's electromagnetic emission

The influence of different power supply arrangements on an IC's EME was investigated by using two different EMC characterization techniques. For the measurement of the conducted emission the 150 Ohm measurement technique as described in the IEC 61967-4 standard was used at the ICs VDD connection. The near magnetic field at the surface of the IC package and its surroundings was characterized with the help of a surface scanning technique as described in the part 3 of this standard [15].

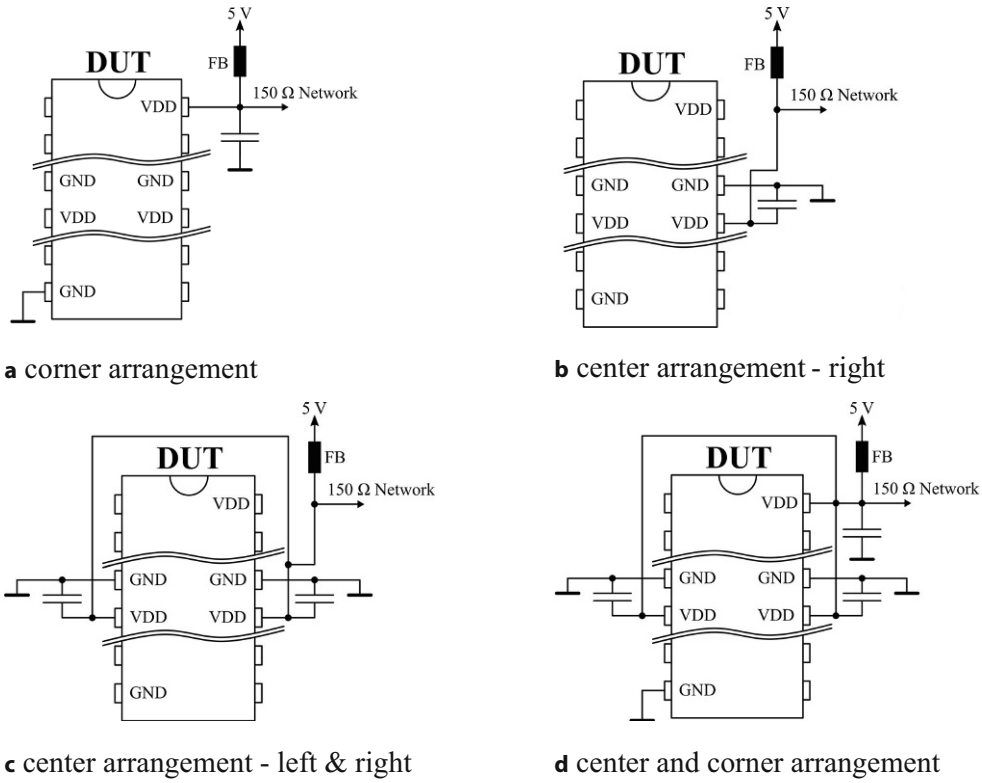
4.1 Configuration of the measurement setup

The DUT was supplied via a 5 V linear regulator, which was decoupled using a ferrite bead (FB). To stabilize the power supply and to reduce the generated electromagnetic emission of the IC a 47 nF SMD decoupling capacitor (X7R, 0603, MLCC) was used between each of the different VDD and GND pins. The 47 nF capacitor was chosen, as it provides the best emission reduction in the desired frequency range. Four power supply arrangements including a corner, single or two-sided center configuration as well as their combinations were tested. The used configurations are presented in Fig. 4. For each of the different power supply configurations the conducted electromagnetic emission at the VDD pin was measured using the 150 Ohm method. In addition the surface scanning techniques was used for the visualization of the distribution of the near magnetic fields in the proximity of the IC.

4.2 Measurement of the conducted emission (150 Ohm method based on IEC 61967-4)

The 150 Ohm method as defined in the IEC 61967-4 standard allows to take repeatable measurements of the conducted EME emitted by an individual pin of an IC [16]. The standard defines this method to be used on I/O or supply pins, which are intended to be connected to PCB traces or cables longer than 10 cm. At this point the main contribution of radiated EMI comes from the antenna formed by the connected wires, rather than from the small antennas formed by the metal traces inside of the IC. Therefore, the IC pins under investigation are connected to a 150 Ω to

Fig. 4 Various power supply arrangements



50 Ω coupling network designed to mimic the typical 150 Ω common mode antenna impedance as specified in the IEC 61000-4-6 standard [17]. Figure 5 shows the coupling network that was connected to the VDD pin of the IC on one side and to an EMI receiver on the other side to measure the conducted EMI of the IC.

The simplicity of the 150 Ohm method allows emission measurements with a high degree of reproducibility, making this method highly suited for characterizing and comparing the emissions of an IC. For this reason, we have decided on using this measurement technique to compare the electromagnetic emission by using different power supply arrangements.

The test setup was implemented on a PCB, which was modified to allow for individual selection of the VDD and GND pins of the DUT. It is equipped with the DUT in the ceramic DIP, the ohmic-capacitive load, as well as the 150 Ω coupling network. Figure 6 shows the PCB and the IC's power supply pins. The PCB layout itself also has a significant impact on the electromagnetic emission of the DUT. To obtain comparable results its overall geometry was not altered during the measurements. The desired power supply arrangements were implemented by selectively bridging cuts within the power supply and GND-plane connections close to the IC's pads.

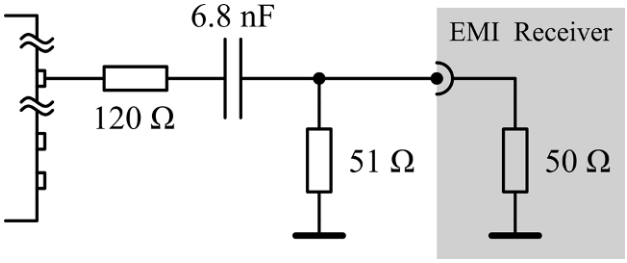


Fig. 5 150 Ω coupling network as defined within IEC 61967-4

4.3 *Measuring the IC's near field emission (surface scan method based on IEC 61967-3)*

The surface scan method, as described in [18], relies on measuring both the electric and magnetic near fields on the surface of an IC. Typically, this involves using specialized electric and magnetic field probes, which are moved automatically in close proximity over the IC package. The induced fields are then analyzed

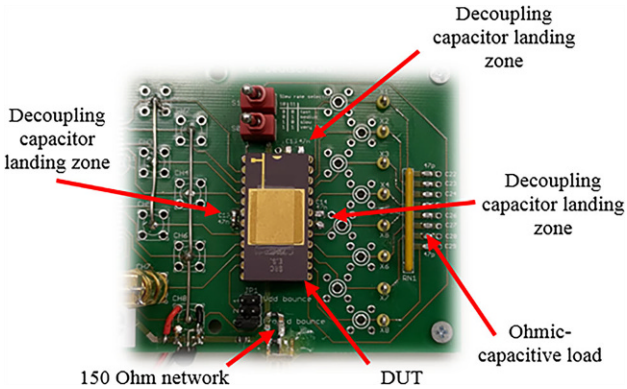


Fig. 6 Implementation of the test setup

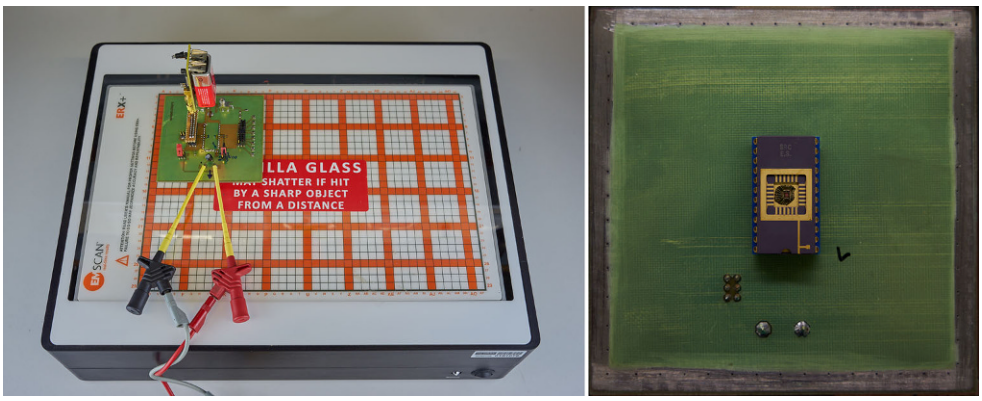


Fig. 7 Implementation of the test setup for the surface scanning method

within a specific frequency range using a spectrum analyzer or EMI-receiver. The resulting data is represented with color-coding and overlaid onto the IC package, providing a visual depiction of field strength at various points on the IC's surface. These visualizations offer design engineers a comprehensive view of near field distribution on the IC surface, helping to identify areas of higher and lower electromagnetic emissions.

The surface scanning system that was used for the investigation presented in the following chapter measures the magnetic field distribution at the surface of PCBs that have to be placed on the scanner's glass surface. It features an integrated spectrum analyzer connected to an array of 1218 magnetic field probes arranged in a grid that can be moved in X- and Y-direction by stepper motors. It is designed to measure magnetic field amplitude emanating from PCBs within a frequency range of 150 kHz to 8 GHz. In Fig. 7 a picture of the used test PCB as well as the measurement setup of the surface scanning system is shown.

In order to characterize the magnetic field distribution a special test PCB was designed, where only the DUT was placed on one side of the PCB. All other components necessary for the operation of the DUT were placed on the other side. The advantage of this PCB is that only the DUT can be placed directly on the scanner and thus the closest possible proximity of the IC to the field probes of the scanner can be achieved. In addition, this arrangement enables that only the near magnetic field of the IC is characterized and no further magnetic fields, which are generated by currents in the additional components, are measured.

The IC was then operated the same way as described for the 150 Ohm method while being placed on the surface scanner. As the surface scan measurements could only be performed at a single frequency at a time, a pre scan was conducted to determine a suitable center frequency for comparing the magnetic field distributions of the different power supply configurations. This was achieved by first performing a frequency scan at the lowest spatial resolution of the surface scanner, which showed the highest mag-

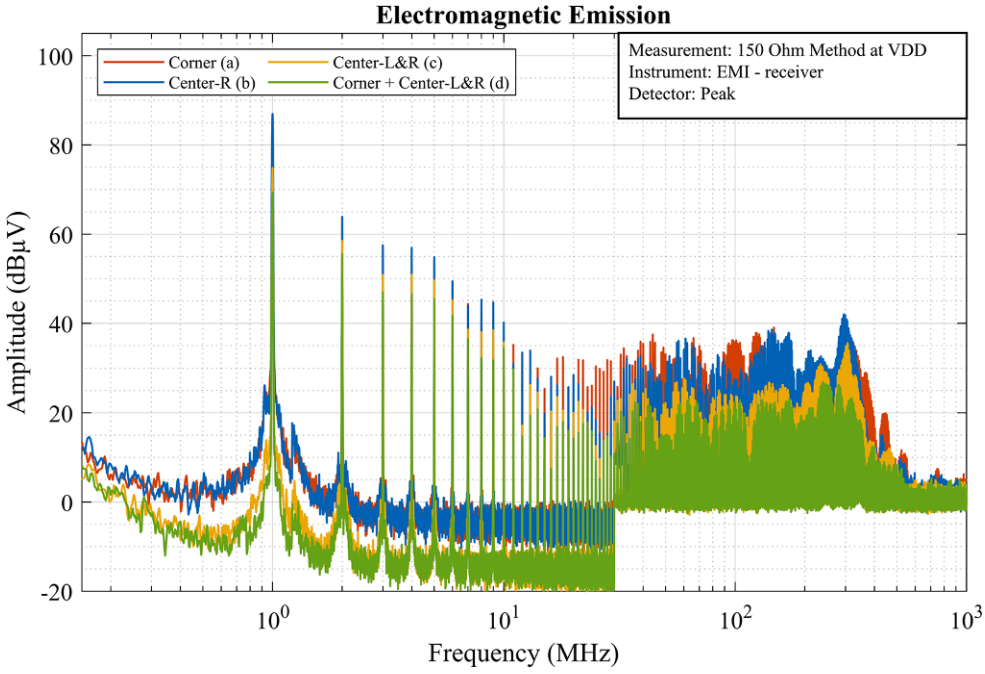


Fig. 8 Result of the conducted emission measurement

netic field magnitude at a frequency of 7 MHz. This frequency was then used as a center frequency for all of the subsequent measurements. The measurements themselves were performed with a resolution bandwidth of 122 kHz and a spatial resolution of 0.94 mm. By using the interleaving option two magnetic field orientations were measured and interleaved by the scanner.

5 Measurement results

In this section, the measurement results of the two measurement methods will be shown and compared against each other. The aim is to find out which power supply arrangement produces the lowest electromagnetic emissions and how large the differences are.

Figure 8 shows the results of the conducted emission measurements of all four different IC supply configurations in an emission plot from 150 kHz to 1 GHz. The switching frequency of 1 MHz and all its harmonics are clearly visible up to the high MHz range. The emission spectrum clearly shows the reduction in emissions due to the use of the decoupling capacitor (especially around its series resonance frequency at ~ 20 MHz). As can be seen, the decoupling capacitor helps to reduce the emission generated by the IC up to about 10–30 MHz, where it still shows capacitive behavior below its series resonance frequency. After that, the parasitic inductance (ESL) of the capacitor itself and especially the loop inductance due to its placement on the PCB start to dominate. This makes the decoupling capacitor less and less effective. At such high frequencies, the results are mainly determined by additional resonances of the entire assembly. This can lead to a significant local increase of EME, as can be observed e.g. around 300 MHz. Such effects can be due to parallel resonances formed e.g. by the die substrate's capacitance to surrounding elements in combination with the parasitic inductances of the bond wires and lead frame of the IC package.

Comparing the result of a corner vs. a center supply arrangement (see Fig. 4 arrangement (a) vs. Figure 4 arrangement (b)), shows similar results in the frequency range up to ~10 MHz. Here the emission spectrum is mainly determined by the value of the decoupling capacitor itself, which in this case remained unchanged. The additional parasitic inductance caused by the corner arrangement has no influence in this frequency range.

However, as can be seen in the higher frequency range there is a significant difference. Here the center power supply arrangement offers lower parasitic inductances and therefore results in lower emissions of the IC. For a better overview of the measurement results and to allow for easier comparison, Fig. 9 only shows the envelopes of the maximum emission spectral lines. The difference can be up to 15 dB at e.g. ~28 MHz and a slight reduction can be seen over a wide frequency range from 10 MHz to 100 MHz. Although the center supply arrangement shows an improvement in this range, it performs worse than the corner supply arrangement in the frequency range around 300 MHz, which is due to resonances caused by the interaction between the PCB and the IC.

For this test IC the power supply of the center right and center left arrangement were designed in a very symmetrical way, therefore the emission of the two center configurations are nearly identical. By using both center arrangements at the same time (arrangement (c) in Fig. 4) the emission can be reduced even further. Comparing the corresponding envelope emis-

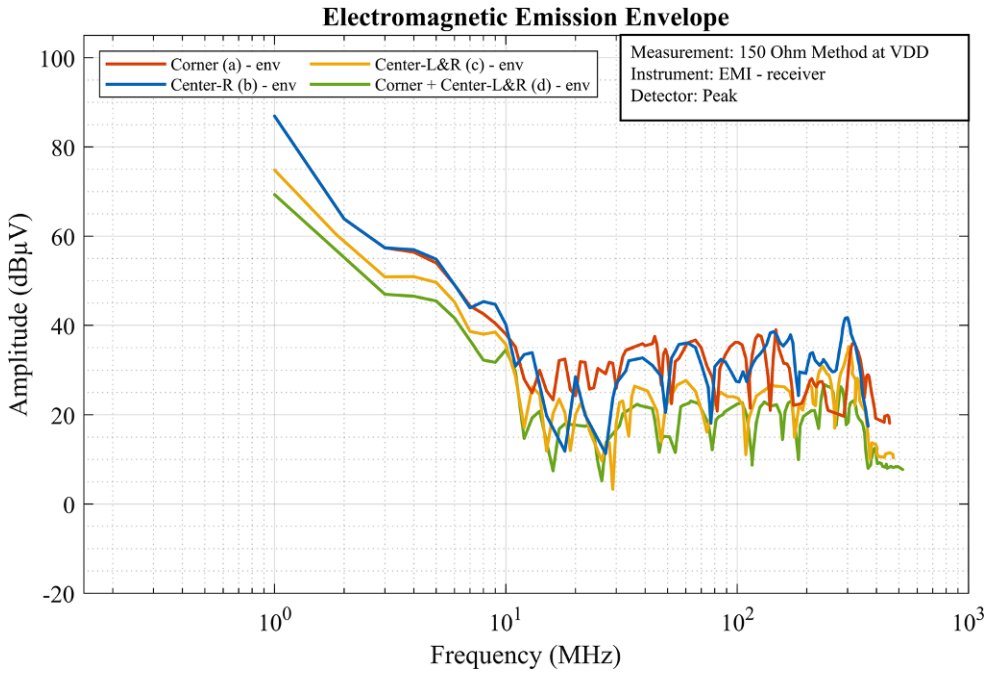
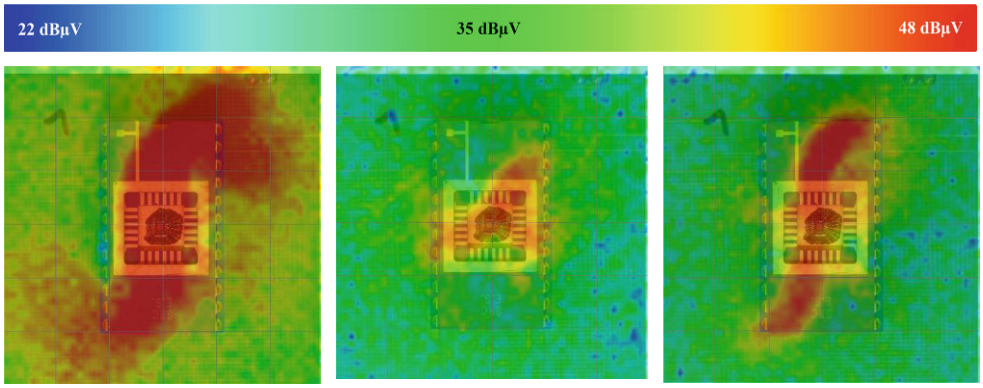


Fig. 9 Envelopes of the conducted emission measurements



a corner arrangement **b** dual sided center arrangement **c** center and corner arrangement

Fig. 10 Near magnetic field distribution for different power supply arrangements

sion plots in Fig. 9 shows a reduction of approximately 10 dB to 15 dB over the whole frequency range. This is to be expected, as the two paralleled supply connections approximately half the package induced parasitic loop inductance. Additionally, the paralleled decoupling capacitors further lower the emission in the low-frequency range, as the total capacitance doubles. In the higher frequency range, they reduce the emission as their total parasitic inductance halves due to their parallel connection.

The lowest emission can be observed when all power supply configurations are combined. In this case three decoupling capacitors act together, providing maximum capacitance as well as minimum parasitic inductance in the power supply. This results in a significant decrease in conducted electromagnetic emissions over the entire frequency range.

Figure 10a shows the magnetic near fields at the surface of the IC package and in the immediate vicinity of a corner supply arrangement with the VDD supply pin in the top right corner and the corresponding GND pin in the bottom left corner. As expected, the large supply loop results in a large area being subjected to increased magnetic near field emissions. Figure 10b shows the magnetic near field of the dual sided center arrangement. The results confirm the hypothesis of lower emissions as they show a significant reduction in magnetic field spreading and magnitude compared to the corner arrangement. This is most likely due to the smaller loop area, as well as the effect of counteracting field orientations due to the symmetrical design of the power supply connections. On the right hand side of the IC, the magnetic field magnitude is higher than on the left hand side of the IC. This is to be expected because on this side the output drivers of the IC are connected to the ohmic-capacitive loads. Therefore, the magnetic fields caused by the dynamic switching currents flowing out of and into the output pins of the IC also contribute to the near magnetic fields that are measured in this area.

Even though the arrangement with all supplies connected resulted in the lowest overall conducted electromagnetic emission, the results presented in Fig. 10c (center and corner arrangement) again show a wider spread of magnetic fields with higher magnitude compared to the dual-sided center arrangement in Fig. 10b. The magnitude is still lower than with a single corner arrangement (Fig. 10a), however, the supply current now distributes between the corner arrangement and the center arrangement, allowing a portion of the current to generate increased magnetic fields due to the larger loop area of the corner arrangement.

6 Conclusion

In this work, two different measurement techniques were used to investigate the influence of the power supply arrangement on the electromagnetic emission of an EMC test chip. In particular, the differences in the emission of corner and center pinning of a dual inline package are compared and discussed. The EMC test chip was operated in a way so that all of its 8 outputs are switching simultaneously with a 1 MHz digital output signal. The generated electromagnetic emission (i.e. harmonics of the 1 MHz signal) extends into the hundreds of MHz range, which provided ideal test conditions for such power supply arrangement investigations. For each of the supply arrangements, a 47 nF decoupling capacitor was used between the respective VDD and GND pins. The measurement results obtained by both measurement techniques (the 150 Ohm method for the conducted emission and the surface scan method for the near magnetic field measurement) showed a significant difference in the electromagnetic emission when different supply arrangements are used. The corner pining arrangement showed in both cases the highest emissions compared to each of the different center arrangements. This is mainly due to the increased power supply loop areas leading to higher parasitic inductances and thus increased conducted emissions and higher near magnetic fields at the surface of the IC package. Using a single center pining arrangement the conducted emission was reduction by about 10 dB over a wide frequency range. This can be attributed to the much smaller power supply loop area caused by the closer pin spacing. Since the pins are now next to each

other, the decoupling capacitor can also be placed optimally. When a dual sided center arrangement is used, the emission can further be lowered by up to 10 dB in the higher frequency range. In this case, the measurement of the magnetic near field also shows the lowest emission because now the center pinning arrangement provides a symmetrical supply causing a portion of the magnetic near field to cancel each other out. Combining all power supply arrangements (corner and dual sided center) resulted in the lowest overall conducted electromagnetic emission with a reduction of up to 20 dB. However, the surface scan results show that this supply configuration results in increased magnetic near fields at the surface of the IC. To reduce the conducted emissions of an IC, it is advisable to use as many power supply pins as possible. However, if the near magnetic fields in the close proximity of the IC should be reduced it is recommended to use a power supply arrangement, which is as symmetrical as possible. Such an arrangement is particularly important for densely packed electronic systems where near field coupling can be a potential cause of interference. These findings confirm the importance of the power supply planning in the IC package design during the development of EMC-compliant ICs.

Acknowledgements This paper is an extended version of "Impact of Power Supply Arrangement on Electromagnetic Emission from ICs" [19] and supported by TU Graz Open Access Publishing Fund.

Funding Open access funding provided by Graz University of Technology.

References

1. Rollin JJ, Areari G, Roy L (1999) EMC performance of IC packages. 1999 IEEE International Symposium on Electromagnetic Compatability. Symposium Record (Cat. No.99CH36261), Seattle. vol 1, pp 44–46 https://doi.org/10.1109/ISEMC.1999.812865
2. Huang NKH et al Electromagnetic emissions from the IC packaging. 2012 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), Taipei, pp 65–68 https://doi.org/10.1109/EDAPS.2012.6469426
3. Xiong W, Jiang M, Zhu M, Zhu B, Lu J (2018) Analysis of electromagnetic shielding of IC package with thin absorbing material coating inside in two different configurations. 2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC), Suntec City, pp 1216–1221 https://doi.org/10.1109/ISEMC.2018.8393982
4. Huang NKH, Jiang LJ, Yu H, Li G, Xu S, Ren H (2012) Fundamental components of the IC packaging electromagnetic interference (EMI) analysis. 2012 IEEE 21st Conference on Electrical Performance of Electronic Packaging and Systems, Tempe, pp 141–144 https://doi.org/10.1109/EPEPS.2012.6457861
5. Merlin M, Fiori F Impact of package parasitics on the EMC performance of smart power SoCs. 2009 European Microelectronics and Packaging Conference, Rimini, pp 1–6
6. Diaz-Alvarez E, Krusius JP (1999) Package and chip-level EMI/EMC structure design, modeling and simulation. 1999 Proceedings. 49th Electronic Components and Technology Conference (Cat. No.99CH36299), San Diego, pp 873–878 https://doi.org/10.1109/ECTC.1999.776285
7. Sudo T, Sasaki H, Masuda N, Drewniak JL (2004) Electromagnetic interference (EMI) of system-on-package (SOP). IEEE Trans Adv Packag 27(2):304–314. https://doi.org/10.1109/TADVP.2004.828817
8. Deutschmann B, Jungreithmair R (2003) Visualizing the electromagnetic emission at the surface of ICs. 2003 IEEE International Symposium on Electromagnetic Compatibility, 2003. EMC'03, Istanbul. vol 2, pp 1125–1128 https://doi.org/10.1109/ICSMC2.2003.1429114
9. Aoyama S, Kawahito S, Yamaguchi M (2006) Fully integrated active magnetic probe for high-definition near-field measurement. 2006 IEEE International Symposium on Electromagnetic Compatibility, 2006. EMC 2006, Portland, pp 426–429 https://doi.org/10.1109/ISEMC.2006.1706340
10. Rauchenecker A, Ostermann T (2019) Influence of different digital power supply layout styles on the EME of Ics with respect to process variations. 2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI), Chambéry, pp 1–4 https://doi.org/10.1109/SaPIW.2019.8781681
11. Senthinathan R, Prince JL (1991) Simultaneous switching ground noise calculation for packaged CMOS devices. IEEE J Solid-State Circuits 26(11):1724–1728. https://doi.org/10.1109/4.98995
12. Sanna A, Graziosi G (2021) IC-package optimization for conducted EME performance: impact of discrete Decoupling capacitors and parasitic inductive effects. 2021 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC), Nusa Dua—Bali, pp 1–3 https://doi.org/10.1109/APEMC49932.2021.9596872
13. Deutschmann B, Ostermann T (2003) CMOS output drivers with reduced ground bounce and electromagnetic emission. ESSCIRC 2004–29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705), Estoril, pp 537–540 https://doi.org/10.1109/ESSCIRC.2003.1257191
14. Deutschmann B, Winkler G, Jungreithmair R (2003) Effects of skewing output driver switching on the electromagnetic emission. 2003 IEEE Symposium on Electromagnetic Compatibility. Symposium Record (Cat. No.03CH37446), Boston. vol 1, pp 236–241 https://doi.org/10.1109/ISEMC.2003.1236598
15. IEC 61967-3:2014, Integrated circuits—Measurement of electromagnetic emissions—Part 3: Measurement of radiated emission—Surface scan method, 2014
16. IEC 61967-4:2020, Integrated circuits—Measurement of electromagnetic emissions Part 4: Measurement of conducted emissions, 1 ohm/150 ohm direct coupling method, 2020

17. IEC 61000-4-6:2023, Electromagnetic compatibility (EMC)—Part 4–6: Testing and measurement techniques—Immunity to conducted disturbances, induced by radio-frequency fields, 2023
18. Slattery K, Cui W (1999) Measuring the electric and magnetic near fields in VLSI devices. Proc. IEEE International Symposium on Electromagnetic Compatibility 1999, Seattle, pp 887–892
19. Deutschmann B, Juch N (2023) Impact of power supply arrangement on electromagnetic emission from ICs. 2023 Austrochip Workshop on Microelectronics (Austrochip), Graz, pp 31–34 https://doi.org/10.1109/Austrochip61217.2023.10285159

B. Deutschmann, received his M.Sc. degree and the Ph.D. degree in telecommunication engineering from the Graz University of Technology/Austria in 1999 and 2002, respectively. After his studies, he worked in the semiconductor industry from 2000 to 2014 on improving the electromagnetic compatibility (EMC) of integrated circuits. In 2014, he returned to academia and moved to Graz University of Technology/Austria as a full professor for "Electronics" and since then heads the Institute of Electronics. His research area is the design of electronic systems and integrated circuits with a special focus on their electromagnetic compatibility. As part of his research activities, he has filed several patents and authored and co-authored numerous papers and technical articles.

N. Juch, is an electrical engineering student at Graz University of Technology. He commenced his university studies in 2017 as a 15-year-old school student. He has since been in close contact with the Institute of Electronics, working on projects and gaining experience in the field of electromagnetic compatibility (EMC) as well as circuit design. After finishing school he formally enrolled as a regular student in the electrical engineering bachelor's program in 2021. He is now a student project employee at the Institute of Electronics, working in the field of electromagnetic compatibility, designing EMC demos, and generating educational content. As a working student in the electronics department of Frickly Systems GmbH, he is actively involved in electronic product design, effectively linking academic research with practical engineering applications.